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**Presidency University**

**Bengaluru**

 **School Of Computer Science and Engineering & Information Science**

**Summer Term End-Term Examinations, Aug 2024**

**Date**: 13 / 08 / 2024

**Time**: 1:00pm -4:00 pm

**Max Marks**: 100

**Weightage**: 50%

**Odd Semester**: 2023 - 24

**Course Code**: CSA2002//BCA2017/ /CSA2022

**Course Name**: Computer Organization

 **Instructions:**

1. *Read the all questions carefully and answer accordingly.*
2. *Do not write any matter on the question paper other than roll number.*

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| **Q.No** | **Questions** | **Marks** | **CO** | **RBT** |
| 1 | a. With a neat diagram, explain Memory hierarchy and its parameters for measuring its performance? | 4 | CO1 | L1 |
| b. Illustrate the Computer systems RISC & CISC architectures. | 6 | CO1 | L2 |
| c. With a neat diagram explain the functional units of computer | 10 | CO1 | L3 |
| **OR** |
| 2 | a. Explain LOAD and STORE operations of memory with steps | 4 | CO1 | L1 |
| b. Compare and contrast different types of computers | 6 | CO1 | L2 |
| c. With a neat diagram explain the connection between processor and memory | 10 | CO1 | L3 |

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| 3 | a. Discuss General Purpose Register (GPR). | 4 | CO2 | L1 |
| b. Write and explain the parameters of a basic performance equation? | 6 | CO2 | L2 |
| c. Registers R1 and R2 of a computer contains the decimal value 1400,1800. What is the effective address of the memory operand in each of the following instructions by considering a memory with word length of 32 bits? i) Store 30(R1),R5 ii) Add #200,R5 iii) Load 100(R1,R2), R5 iv) Mul -(R2), R5 v) Sub LocA, R | 10 | CO2 | L3 |

**OR**

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| 4 | a. Define Subroutine? Explain subroutine nesting with example | 4 | CO2 | L1 |
| b. With a suitable example, describe the different types of instruction formats | 6 | CO2 | L2 |
| c. Discuss the factors that affect the performance of the computer. Let a processor operates by a frequency 10MHz and it executes a typical program in which 50% are register referenced instruction, 30% are memory reference instructions and 20% are branch instructions. Register referenced instruction, memory reference instructions and branch instructions take 4, 8 and 6 clock cycles respectively. Find out the total time taken by the processor to execute the program | 10 | CO2 | L3 |

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| 5 | a. Explain I/O mapping methods with suitable diagram? | 4 | CO3 | L1 |
| b. List and explain different types of ROM? | 6 | CO3 | L2 |
| c. With a neat diagram, explain single bus organization?  | 10 | CO3 | L3 |

**OR**

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| 6 | a. Write the steps to show how interrupts are handled?  | 4 | CO3 | L1 |
| b. Name the three systems used for representing numbers. Discuss each system with relevant example | 6 | CO3 | L2 |
| c. Write the control sequence for execution of a complete instruction for single bus organization? | 10 | CO3 | L3 |

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| 7 | a. Write an Algorithm to carry out Multiplication using Booth Algorithm? | 4 | CO4 | L1 |
| b. Explain DMA with a neat diagram? | 6 | CO4 | L2 |
| c. Explain 4-bit carry look ahead adder with a neat diagram. Write all the carry equations and find the delay for all carry and sum bits. | 10 | CO4 | L3 |

 **OR**

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| 8 | a. Define cache memory and explain locality of references? | 4 | CO1 | L1 |
| b. Detail the Execution of a Complete instruction with the sequence of elementary operations required to execute the following instruction: ADD R3, R1 using single bus organization | 6 | CO1 | L2 |
| c. Perform multiplication on the following using sign extension and Booth’s Algorithm for 12 \* -18 | 10 | CO1 | L3 |

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| 9 | a. With an example explain parameter passing through registers? | 4 | CO1 | L1 |
| b. Differentiate between programmed I/O and Interrupt driven I/O? | 6 | CO1 | L2 |
| c. Write the steps and flow chart for restoring division algorithm? | 10 | CO1 | L3 |

**OR**

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| 10 | a. Draw the flowchart for Multiplication of positive numbers and steps with an example.  | 4 | CO2 | L1 |
| b. Explain 4 bit carry look ahead adder/addition with suitable diagram? | 6 | CO2 | L2 |
| c. Perform restoring Division on the 15/4 | 10 | CO2 | L3 |