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**Presidency University**

**Bengaluru**

**SCHOOL OF ENGINEERING**

**SUMMER TERM END TERM EXAMINATION AUG-2024**

**Summer Term**: August 2024

**Course Code** : ECE2002 / ECE2006

**Course Name** : Digital Electronics

**Program** : BTech

**Date** : 05 August 2024

**Time** : 9:30 am – 12:30 pm

**Max Marks** : 100

**Weightage** : 50 %

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculators are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

**Part A [Memory Recall Questions]**

**ANSWER ANY 4 QUESTIONS (4Q x 5M = 20M)**

1. Fill in the blanks.

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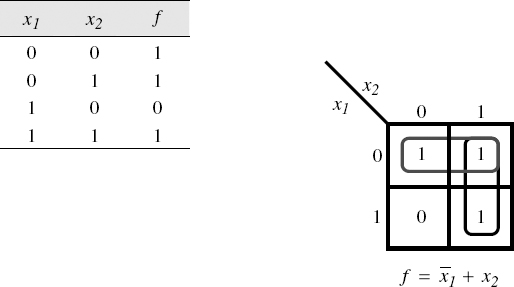
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(CO1) [Knowledge]

1. Draw the template of 2 variable K-map and obtain an expression for the variables x1 and x2 shown in truth table below.

(CO1) [Knowledge]

1. Implement the basic gate OR using NAND gates only.

(CO1) [Knowledge]

1. Differentiate between combinational and sequential circuit.

(CO3) [Knowledge]

1. Draw the symbol and truth table of AND gate and NAND gate.

(CO1) [Knowledge]

1. Explain Associative law of Boolean algebra.

(CO1) [Knowledge]

**Part B [Thought Provoking Questions]**

**ANSWER ANY FOUR QUESTIONS (4Q x 10M = 40M)**

1. Sheetal targets to reduce the number of gates in a given circuit, thereby simplifying a complex circuit reducing the cost, size and area of the integrated circuit. Sheetal is given an expression ∑m(0,2,3,6,7,8,10,12,13). Obtain a simplified expression so as to achieve her target.

(CO1) [Comprehension]

1. A Karnaugh map or a K-map refers to a pictorial method that is utilised to minimise various Boolean expressions without using the Boolean algebra theorems along with the equation manipulations. A Karnaugh map can be a special version of the truth table. Using K-map simplify the given Boolean expression f=∑m(0,2,3,6,7) + d(8,10,11,15).

(CO1) [Comprehension]

1. The combinational circuit that changes the binary information into 2N output lines is known as Decoder. The binary information is passed in the form of N input lines. Design full subtractor using 3:8 line decoder.

(CO2) [Comprehension]

1. Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. Highlight the major differences in the block diagram of SISO, SIPO, PISO, PIPO shift registers.

(CO3) [Comprehension]

1. A De-multiplexer (DEMUX) is a combinational circuit that has only 1 input line and 2N output lines. On the basis of the values of the selection lines, the input will be connected to one of these outputs. Higher order DEMUX can be built using lower order DEMUXs. Design 1:8 DEMUX using 1:2 DEMUXs.

(CO2) [Comprehension]

**Part C [Problem Solving Questions]**

**ANSWER ANY 2 QUESTIONS (2Q x 20M = 40M)**

1. A multiplexer in digital electronics is known as a data selector. It is a Combinational Logic Circuit having multiple input lines, one output line, and many select/control lines. Design 2x1, 4x1, and 8x1 multiplexer using basic gates such as AND, NOT and OR gates. Explain the working of these multiplexers using truth table and output equations.

(CO2) [Application]

1. T Flip-Flop is a single input logic circuit that holds or toggles its output according to the input state. Toggling means changing the next state output to complement the current state. T is an abbreviation for Toggle. Explain T flip flop with the help of symbol, logic diagram, truth table, characteristic table, characteristic equation, excitation table.

(CO3) [Comprehension]

1. Counters are sequential circuits which change their pre-defined states with the help of clock pulses. They are constructed with flip flops and logic gates. Design 3-bit down counter using JK flip flop.

(CO3) [Application]