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 PRESIDENCY UNIVERSITY,

 BENGALURU

SCHOOL OF COMPUTER SCIENCE AND ENIGINEERING

SUMMER TERM END TERM EXAMINATION – AUG 2024

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| **Semester : Summer Term** | **Date : 14-08-2024** |
| **Course Code : ECE2007**  | **Time : 1:00 PM-4:00PM** |
| **Course Name : DIGITAL DESIGN** | **Max Marks : 100** |
| **Program : B.TECH /BCA** | **Weightage: 50%** |
| **PART A** |
|  **ANSWER ANY 3 QUESTIONS 3Q X 5M=15M** |
| 1 | NAND and NOR are Universal gates, which means that any other logic gates can be implemented using them. Draw the XOR and X-NOR using 5 NAND gates. | (CO 1) | [Knowledge] |
| 2 | Multiplexer is a combinational circuit used as a parallel -serial converter, which has multiple input line and a single output line. Write the truth table and derive the basic gate logic using 2x1 MUX. | (CO 2) | [Knowledge] |
| 3 | An adder, or summer, is a digital circuit that performs addition of numbers. Implement a half adder circuit using XOR gates and write its expression. | (CO 2) | [Knowledge] |
| 4 | A *Magnitude Comparator* is a digital comparator which has three output terminals. Design a 1-bit comparator using basic gates. | (CO 2) | [Knowledge] |
| 5 | When using static gates as building blocks, the most fundamental latch is the simple SR latch. Construct and Implement SR latch using NAND gates. | (CO 3) | [Knowledge] |
| **PART B** |
|  **ANSWER ANY 2 QUESTIONS 2Q X 20M=40M** |
| 6 | An encoder in digital electronics is a specialized circuit that transforms binary inputs into a distinct binary code. Design a Octal to binary encoder circuit using 4 input OR gate and write its truth table. | (CO 2) | [Comprehension] |
| 7 | Flipflop and Latches are the fundamental building blocks of digital electronic system. For a JK flipflop, draw the logic symbol, circuit diagram and derive the characteristic table, characteristic equation and the excitation table. | (CO 3) | [Comprehension] |
| 8 | In many domestic application (like Digital clock, Timers.) Up Counter logic circuits are used frequently. Using State - table and K-map design a 3 bit counter using JK flip flop to count the decimal number from 0 to 7 in binary form. | (CO 3) | [Comprehension] |
| **PART C** |
|  **ANSWER ANY 3 QUESTIONS 3Q X 15M=45M** |
| 9 | Mr. Joe intends to use K-map to minimize the Boolean expression f= $\sum\_{}^{}m\left(0,1,2,4,7,8,9,10,12\right)+d\left(3,6,13,15\right). $ Help him to implement the expression with minimum sum of product terms using basic gates .  | (CO 1) | [Application] |
| 10 | Given a POS Boolean expression is F= (B+C’+D’)(A’+B’+C+D)(A+B’+C’+D’).1. Convert Standard POS into Canonical POS.

Using K-map Find the simplified SOP expression and implement using gates.  | (CO 1) | [Application] |
| 11 | The designer can design a Full Adder using two Half adder and one basic gate. From the full adder truth table, Using K-map derive the needed equation and design a full adder circuit using Half adders and one OR gate. | (CO 2) | [Application] |
| 12 | Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit. Design a 2 bit Counter and simplify the expression using K-Map and implement using JK flipflop. | (CO 3) | [Application] |