

PRESIDENCY UNIVERSITY **BENGALURU**

SCHOOL OF ENGINEERING

TEST - 1

Even Semester: 2018-19

Course Code: ECE 101

Course Name: Elements of Electronics Engineering

Programme & Sem: B.Tech (Chemistry Cycle) & II Sem

Date: 06 March 2019

Time: 1 Hour

Max Marks: 40

Weightage: 20%

Instructions:

Read the question properly and answer accordingly. (i)

(ii) Question paper consists of 3 parts.

Scientific and Non-programmable calculators are permitted. (iii)

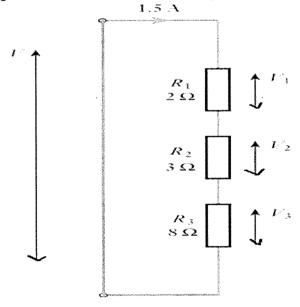
This question paper contains two pages. (iv)

Part A

Answer all the Questions. Each question carries four marks.

(3Qx4M=12)

1. Calculate the voltage across Resistor R1, supply voltage V and equivalent resistance of the circuit shown in figure and hence calculate the power dissipated by resistor R2.



- 2. Draw the symbol of npn and pnp transistors. Indicate the terminal voltages and currents.
- 3. Explain Ideal diode approximation.

P.T.O

Part B

`Answer **both** the Questions. **Each** question carries **eight** marks.

(2Qx8M=16)

- 4. a) What is the purpose of a DC load line? Draw a DC load line for a series circuit made up of DC supply voltage Vs, a resistor R and a diode?
 - b) Derive the expression for Vo(rms) of Half Wave Rectifier.
- 5. Draw the VI characteristics of pn junction diode. Explain the following parameters
 - a) Reverse Breakdown voltage
 - b) Forward voltage drop
 - c) Knee voltage
 - d) Dynamic resistance
 - e) Reverse saturation current
 - f) Maximum forward current

Part C

Answer **both** the Questions. **Each** question carries **six** marks.

(2Qx6M=12)

- 6. Draw the circuit diagram & explain Full wave rectifier with capacitor filter with necessary waveforms.
- 7. a) A Si Diode working at 75°C, with the reverse saturation current 10 μ A, forward current of 100mA, and η =2. Determine the forward voltage required to be applied to the diode.
 - b) Differentiate between Avalanche Breakdown and Zener Breakdown.



PRESIDENCY UNIVERSITY BENGALURU

SCHOOL OF ENGINEERING

TEST - 2

Even Semester: 2018-19

Date: 15 April 2019

Course Code: ECE 101

Time: 1 Hour

Course Name: Elements of Electronics Engineering

Max Marks: 40

Program & Sem: B.Tech & II Sem (Chemistry cycle)

Weightage: 20%

Instructions:

(i) Read Questions carefully and answer accordingly

(ii) Scientific and Non- programmable calculators are permitted

(iii) This question paper contains two pages

Part A

Answer all the Questions. Each question carries four marks.

(3Qx4M=12M)

- 1. With a neat diagram, explain the working of n-p-n transistor.
- 2. Fill in the blanks:

SL.	Parameters	Current Gain formula
No.		
1.	CE	
2.	СВ	
3.	CC	
4.	Condition:- BE Junction:Forward Bias,	Region of Operation:-
	BC Junction: Reverse Bias	

3. A transistor has $I_B=100\mu A$, $I_C=2mA$. Find (i) β (ii) α (iii) I_E

Part B

Answer both the Questions. Each question carries eight marks.

(2Qx8M=16M)

4. For a transistor input terminal is Base and output terminal is Collector. Identify the transistor configuration, draw the circuit, and explain input and output characteristics, mention the regions of operation.

5. For the fixed-bias configuration shown in figure 1, Find I_{BQ} , I_{CQ} , V_{CEQ} , also determine the two points of the DC load line and plot DC Load line. Assume $V_{BE} = 0.7V$

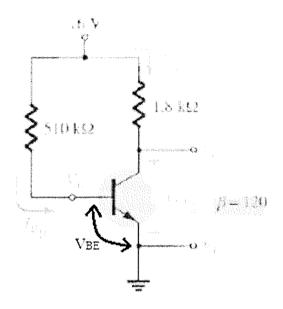


Figure 1

Part C

Answer both the Questions. Each question carries six marks.

(2Qx6M=12M)

- 6. (a) Convert (123)₁₀= ()₂= ()₁₆
 - (b) Find Complements for the following:
 - (i) 1's complement of (110011000011)₂
 - (ii) 2's complement of (1011001)₂
- 7. (a) Perform 1's complement subtraction for following numbers: (11101)₂ (11000)₂
 - (b) Perform binary addition of (110011)₂ and (10101)₂

Roll No.						



PRESIDENCY UNIVERSITY **BENGALURU**

SCHOOL OF ENGINEERING

SUMMER TERM / MAKE UP END TERM EXAMINATION

Semester: Summer Term 2019

Date: 24 July 2019

Course Code: ECE 101

Time: 2 Hours

Max Marks: 80

Course Name: Elements of Electronics Engineering

Program & Sem: B.Tech & I Sem (2017 & 2018 Batch)

Weightage: 40%

Instructions:

Read the question properly and answer accordingly. (i)

Question paper consists of 3 parts. (ii)

(iii) Scientific and Non-programmable calculators are permitted.

Part A

Answer **all** the questions. **Each** question carries **five** marks.

(4Qx5M=20)

- 1. Simplify and Implement Following Using AND-OR logic F= (1,3,5).
- 2. State the formulae for alpha, Beta. If for a silicon transistor, alpha is 0.95, $I_E = 5$ mA. Find I_C and I_B. Neglect I_{CBO}.
- 3. Why NAND gate is known as universal gate? Explain with proper diagrams how you can implement NOT gate and AND gate using NAND gate.
- 4. Match the following.

COLUMN A	COLUMN B
1. CB Configuration	A. Input is Base Output is Collector
2. CE Configuration	B. Input is Base Output is Emitter
3. CC Configuration	C.Junction1 Forward Bias, Junction2 Reverse bias
4. Active Region	D. Both junctions Forward bias
5. Saturation Region	E. Input is Emitter Output is Collector

Part B

Answer all the questions. Each question carries ten marks.

(4Qx10M=40)

5. Discuss in brief all the logic gates with proper symbols and truth-table.

- 6. A) State Demorgan's theorem and prove with truth table method. (6 Marks)
 - B) Draw symbols for NPN and PNP transistor. (4Marks)
- 7. Explain the application of transistor as an amplifier with proper diagrams.
- 8. State the reasons why Common emitter configuration is mostly preferred. Explain the common emitter configuration of Transistor with proper well labeled diagrams.

Part C

Answer both the questions. Each question carries ten marks.

(2Qx10M=20)

- 9. Explain the block diagram of communication system. Define each and every block with proper explanation.
- 10. Define Modulation. State why there is a need of modulation. Explain Frequency Modulation in details.



	l .	1	[l	l	l	!		 1
Roll No										
										Ė

PRESIDENCY UNIVERSITY BENGALURU

SCHOOL OF ENGINEERING

MAKE UP EXAMINATION JULY 2019

Semester: Summer Term 2019

Date: 22 May 2019

Course Code: ECE 101

Time: 3 Hours

Course Name: Elements of Electronics Engineering

Max Marks: 80

Program & Sem: BTech & II Sem (EVEN)(2018 Batch)

Weightage: 40%

Instructions:

- (i) Read the question properly and answer accordingly.
- (ii) Question paper consists of 3 parts.
- (iii) Scientific and Non-programmable calculators are permitted.
- (iv) Use of mobile phones and other electronic aids is strictly prohibited.

Part A

Answer all the Questions. Each question carries one mark.

(20Qx1M=20)

- 1. Multiple choice questions.
 - I. The most Commonly used semiconductor is
 - a) Germanium
 - b) Silicon
 - c) Boron
 - d) Galium
 - II. In semiconductor Current conduction is due to
 - a) Holes
 - b) Electrons
 - c) Neutral charges
 - d) Both holes and Electrons
- III. A reverse biased PN junction constitutes
 - a) Only Forward Bias current
 - b) Only Reverse bias Current
 - c) Both of the above
 - d) Zero Current
- IV. A reverse Current is generally in _____ amperes
 - a) Milli
 - b) Micro
 - c) Nano
 - d) Pico
- V. A zener diode is generally used as
 - a) Voltage divider
 - b) Switch
 - c) Amplifier
 - d) Voltage Regulator

VI.	A Half wave rectifier consists of	Diodes.
	a) Two	
	b) One	
	c) Four	
	d) None of the above	
\ /II	,	iunctions
VII.	A transistor has PN	junctions.
	a) Two	
	b) Three	
	c) Four	
	d) More than five	
VIII.	Most commonly used transistor co	nfiguration is
	a) Common Emitter	
	b) Common Collector	
	c) Common Base	
	d) NONE	
IX.	Collector base junction is	in Active region.
	a) Forward biased	
	b) Reverse biased	
	c) First Reverse then Forward bia	ased
	d) Insufficient data	
Χ.	BJT is device	
	 a) Only TWO Junctions 	
	b) Only Bipolar	
	c) Only Switching	
	d) All	
XI.	Match the pairs (Q11- Q15)	
	I. Lightly doped	a) Collector
	II. Largest width	b) P-N junction Diode
	III. Alpha	c) Base
	IV. Beta	d) Generally have higher values starting from 200.
	V. Avalanche Breakdown	e) Always less than or equal to 1.
XII.	Fill in the blanks (Q16- Q20)	
	•	
	a) 8085 have an ALU which can Pr	ocess bits at a time.
	b) Semiconductors can be cons	idered to inhibit the properties of at room
	temperature	
	c) Holes can be defined as absent	ce of
		ed in series are connected across a lamp as a load. With the
	help of Digital logic it is represen	
	e) Involution law is also known as	Negation law.
	of involution law to also known do	

Part B

Answer all the Questions. Each question carries four marks.

(5Qx4M=20)

- Explain with neat circuit diagram and waveforms how transistor can be used to amplify Current. Also Explain Which Configurations among common terminals is used for amplifier.
- 3. Define Beta. Derive Alpha in terms of Beta with suitable steps.
- 4. Explain with the help of suitable diagrams how we can Classify materials based on the energy bands. Use suitable values wherever necessary.
- 5. Define Modulation. State and Elaborate the various reasons for Need of Modulation and also Explain with Example how antenna length is Reducing with increasing carrier frequency.
- 6. State and Prove Associative law.

Part C

Answer all the Questions. Each question carries ten marks.

(4Qx10M=40)

- 7. Explain In brief each block of Communication System block diagram with neat and well labelled diagram. Also state Real life example where Frequency Modulation is used.
- 8. Sketch the Architecture of Microprocessor 8085 and Explain the following Blocks.
 - A) ALU B) Stack pointer C) Program counter D) Instruction register
 - E) Interrupt control F) Timing and control unit G) Register set
- Draw the logic symbol, expression and truth table for the following logic gates
 A) AND G) Ex-NOR C) OR D) NAND E) NOR F) Ex-OR.
 Also Realize NOT gate using NAND GATE.
- 10. Answer all subparts.
 - Simplify and Implement Following Using AND-OR LOGIC.
 F=(1,3,5)
 - II. Perform Logical Addition and Binary addition for the following.11110+10001. Also write table for both Additions.



Roll No					
NIVERS	ITY				
RU					



(vii) In a transistor

PRESIDENCY UNIVERSITY BENGALURU

SCHOOL OF ENGINEERING

TAID TERM FINAL EXAMINATION	1
END TERM FINAL EXAMINATION	
Even Semester: 2018-19	Date : 22 May 2019
Course Code: ECE101	Time: 3 Hours
Course Name: Elements of Electronics Engineering	Max Marks: 80
Program & Sem: B. Tech & II Sem (Chemistry Cycle)	Weightage: 40%
Instructions: (i) Answer all the questions in Part A, Part B and Part C	
(i) Thrower an are queenene in the investment of	
Part A	
Answer all the following multiple-choice questions.	(10Qx1M=10N
Ripple factor of half wave rectifier is	
A. 1.414	
B. 1.21	
C. 1.3	
D. 0.4	
(ii) When P-N junction is in forward bias, by increasing the battery volta	iae
A. Circuit resistance increases	90
B. Current through P-N junction increases	
C. Current through P-N junction decreases	
D. None of the above happens	
A P-N junction	
A. Has low resistance in forward as well as reverse direction	
B. Has high resistance in forward as well as reverse direction	IIS
C. Conducts in forward direction onlyD. Conducts in reverse direction only	
(iv) In a PN junction when the applied voltage overcomes the potential of the poten	ential, the diode current is large,
which is known as	,
 A. Depletion, negative bias 	
B. Reverse, reverse bias	
C. Resistance, reverse bias	
D. Barrier, forward bias	
(v) A transistor has	
B. two pn junctions	
C. three pn junctions	
D. four pn junctions	
(vi) The base of a transistor is doped	
A. heavily	
B. moderately C. lightly	
D. none of the above	

(viii) Output will be a LOW for any case when one	or more inputs are zero for :	
A. OR gate B. NOT gate		
C. AND gate		
D. NOR gate		
(ix) When an input signal 1 is applied to a NOT ga	ate, the output is	
A. 0 B. 1		
C. Either 0 & 1		
D. None of the above		
(x) The output of an AND gate with three inputs, A	A, B, and C, is HIGH when	
A. A=1, B=1 and C=0		
B. A=0, B=0 and C=0		
C. A=1, B=1 and C=1		
D. A=1, B=0 and C=1		
Answer all the following questions	(5	5Qx1M=5M)
(i) The sum of 11101 + 10111 equals	•	, 4,,,,,,
(ii) The relation between β and α is		
(iii) Conversion of binary 01001110 to decimal is	·	
(iv) If the input to a NOT gate is A and the output		
(v) A P-N junction diode conducts in biase	ed condition.	
Match the following:	(5	Qx1M=5M)
		,
Α	В	
1. In a half wave rectifier, current flows	a. when it is in cut off region	
2. A transistor acts as an open switch.	b. in half of the input signal	
3. A transistor operates as a closed switch.4. The value of radix in binary number system is	c. amplitude. d. when it is in saturated region	
5.In amplitude modulation the signal is	e. two	
modulated with respect to	e. two	
modulated Will Teopera to		
Part B		
swer all the Questions. Each question carries four ma	arks. (50	Qx4M=20M)
	(

Ans

- 4. Explain working of half wave rectifier with neat circuit diagram and waveforms.
- 5. With neat diagram, explain the forward biased P-N junction diode.
- 6. Explain transistor as an amplifier.

2.

3.

- 7. Define Amplitude modulation and draw the waveforms.
- 8. State the laws of Boolean algebra (Commutative law, associative law, distributive law), prove using truth table method.

Part C

Answer all the Questions. Each question carries ten marks.

(4Qx10M=40M)

- 9. Write the logic symbol, expression and truth table for the following logic gates c. OR d. NOR
 - a. NOT
- b. AND
- 10. State and explain De Morgan's theorem for 2- variables.
- 11. Explain with a neat diagram the block diagram of communication system.
- 12. Draw the architecture of 8085 microprocessor and explain the following blocks a) ALU b) Stack pointer c) Program counter and d) Instruction Register and decoder