Roll No												

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

SUMMER TERM / MAKE UP END TERM EXAMINATION

Semester: Summer Term 2019 | **Date**: 22 July 2019

Course Code: CSE 202 | **Time**: 2 Hours

Course Name: Digital Design | **Max Marks**: 80

Program & Sem: B.Tech & III Sem (2016 & 2017 Batch) | **Weightage**: 40%

Instructions:

(i) Read the question properly and answer accordingly and to the point.

(ii) Question paper consists of 3 parts.

(iii) Sci*entific and Non-programmable calculators are permitted.*

Part A

Answer **all** the Questions. **Each** question carries **ten** marks. (3Qx10M=30M)

1. State and Prove De-Morgan's Theorem. Realize fundamental gates using NOR gates.
2. Minimize the following Boolean function using K - map method

   $F(A,B,C,D) = \Sigma m(1,3,4,5,9,11,14,15) + \Sigma d(2,6,7,8)$

   Realize the resultant expression using NAND gates.
3. Define Multiplexer. With a neat circuit diagram, explain the working principle of 16:1 Multiplexer.

Part B

Answer **all** the Questions. **Each** question carries **fifteen** marks. (2Qx15M=30M)

4. Apply Quine Mc-Clusky method to find the essential prime implicants for the Boolean expression $F(A,B,C,D) = \Sigma m(0,1,2,3,10,11,12,13,14,15)$
5. Explain the different representations of SR, D and JK Flip-flops.

Part C

Answer **both** the Questions. **Each** question carries **ten** marks. (2Qx10M=20M)

6. Design a mod-5 counter using JK-Flip-flops.
7. With a neat block diagram, explain the working of a Master-Slave JK Flip-flops.