Roll No.											

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST - 1

Even Semester: 2018-19 | **Date**: 05 March 2019

Course Code: CSE 205 | **Time**: 1 Hour

Course Name: Computer Organization and Architecture | **Max Marks**: 40

Programme & Sem: B.Tech (CSE) & IV Sem | **Weightage**: 20%

Instructions:

(i) Read the questions and answer accordingly.

(ii) Question Paper consists of 3 parts.

Part A

Answer **all** the Questions. **Each** question carries **five** marks. (2Qx5M=10)

1. Explain the types of Byte Addressability with suitable diagram:-
2. Write and explain each parameter of the Basic Performance Equation.

Part B

Answer **all** the Questions. **Each** question carries **ten** marks. (2Qx10M=20)

3. Explain the following types of addressing modes with example.

   i) Absolute mode

   ii) Immediate mode

   iii) Relative Addressing

   iv) Base with index mode

   v) Base with index and offset

4. With a neat diagram explain the connection between the processor and memory.

Part C

Answer the Question. Question carries **ten** marks. (1Qx10M=10)

5. a) Using 4 - bit signed numbers **add** the following and check for overflow?

   i) +2 and -3
   ii) -4 and -6
   iii) -6 and +4

   b) Using 4 - bit signed numbers **subtract** the following and check for overflow?

   i) +7 and +4
   ii) -7 and +1

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GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST - 2

Even Semester: 2018-19 | **Date**: 15 April 2019

Course Code: CSE 205 | **Time**: 1 Hour

Course Name: Computer Organization and Architecture | **Max Marks**: 40

Program & Sem: B.Tech & IV Sem | **Weightage**: 20%

Instructions:

(i) *Read the question properly and answer accordingly.*

(ii) *Question paper consists of 3 parts.*

(iii) Scientific and Non-programmable calculators are permitted.

Part A

Answer **both** the Questions. **Each** Question carries **ten** marks. (2Qx10M=20)

1. With a neat diagram explain the Single Bus Processor Architecture. List the control sequence required for fetching the instruction Add (R3), R1.
2. With neat block diagram, explain the Internal Organization of 16 x 8 memory chip. Find the minimum number of external pins for this memory chip.

Part B

Answer the Question. Question carries **ten** marks. (1Qx10M=10)

3. What is Interrupt Latency? Explain the three possibilities of Enabling and Disabling Interrupts.

Part C

Answer the Question. The Question carries **ten** marks. (1Qx10M=10)

4. What is the drawback of ripple carry adder? Design a 4 bit Carry Look-Ahead Adder by clearly stating the Boolean equations of the look ahead carry generation. Specify the gate delay required for generating the carry-out signal.

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SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Even Semester: 2018-19 | **Date**: 21 May 2019

Course Code: CSE 205 | **Time**: 3 Hours

Course Name: Computer Organization and Architecture | **Max Marks**: 80

Program & Sem: B.Tech & IV Sem | **Weightage**: 40%

`structions:

(i) Read the question properly and answer accordingly.

(ii) Question paper consists of 3 parts.

(iii) Scientific and Non-programmable calculators are permitted.

Part A

Answer **all** the Questions. **Each** question carries **one** mark. (20Qx1M=20M)

1. Answer the following MCQs / Fill in the blanks:

i. A very large and expensive computer capable of supporting hundreds or even thousands of users simultaneously is called

a. Microcomputer b. Mainframe

c. Server d. Minicomputer

ii. The number of bits in each word is called as

a. Bit length b. Word length c. Bit word d. word bit

iii. The three types of buses connected to CPU are:

a. Data, address, control b. Data, system, address

c. Address, control, memory d. Fetch-code, control, execution.

iv. Which instruction type has the format Operation Source/Destination

a. Zero Address Instruction b. One Address Instruction

c. Two Address Instruction d. Three Address Instruction

v. The addressing mode in which the address of the operand is given explicitly in the instruction is called as

a. Immediate mode b. Register mode

c. Absolute mode d. Index mode

vi. During the execution of a program which gets initialized first?

a. MDR b. IR c. PC d. MAR

vii. The PC gets incremented

a. After the Instruction decoding b. After the IR instruction gets executed

c. After the fetch cycle d. None of the above

viii. The type of memory assignment used in Intel processors is _____

a. Little Endian b. Big Endian

c. Medium Endian d. None of the above

ix. In subroutines, the order in which the return addresses are generated and used is_____

a. LIFO b. FIFO

c. Random d. Highest Priority

x. The registers, ALU and the interconnection between them are collectively called as _____

a. Process Route b. Information trail

c. Information path d. Data Path

xi. Coordination and control of the activities among the functional units is done by the

a. Key board b. ALU

c. Control unit d. Memory

xii. Address of next instruction to be fetched and executed is stored in

a. PC b. MAR

c. IR d. MDR

xiii. The effectiveness of the cache memory is based on the property of _____

a. Locality of reference b. Memory Localization

c. Memory size d. None of the mentioned

xiv. The instructions like MOV or ADD is called as

a. Operators b. Commands

c. Op-code d. None of the above

xv. The fastest data access is provided using _____

a. Caches b. DRAMs

c. SRAMs d. Registers

xvi. The number of external pins required for 32 x 16 memory configuration is _____

xvii. The IEEE 754 Floating point single precision representation uses _____ bits for exponent field.

xviii. The ALU makes use of _____ to store the intermediate results.

xix. _____ Bus structure is usually used to connect I/O devices.

xx. The addressing mode, which uses the PC instead of a general purpose register is _____

Part B

Answer **all** the Questions. **Each** question carries **ten** marks. (3Qx10M=30M)

2. Explain Booth algorithm. Apply Booth algorithm to multiply the signed numbers +13 and -6
3. a. Discuss five stage instruction pipeline with proper illustration.
   b. Multiply +18 and -7 using bit-pair recoding.
4. With neat relevant diagrams, explain Flynn's classification.

Part C

Answer **all** the Questions. **Each** question carries **ten** marks. (3Qx10M=30M)

5. Explain IEEE standards for floating point numbers. Represent 1259.125 in single precision format.
6. What is Pipeline Hazard? With a neat diagram and an example, explain structural and data hazard.
7. Write the steps involved in performing restoring division algorithm. Given A = 10101 and B= 00100 perform A/B using restoring division algorithm.

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SUMMER TERM/ MAKE UP END TERM EXAMINATION

Semester: Summer Term 2019 | **Date**: 22 July 2019

Course Code: CSE 205 | **Time**: 2 Hours

Course Name: Computer Organization and Architecture | **Max Marks**: 80

Program & Sem: B.Tech, V & IV Sem (2015 & 2016 batch) | **Weightage**: 40%

Instructions:

(i) ***Non- Programmable calculators are allowed***

Part A

Answer **all** the Questions. **Each** question carries **five** marks. (4Qx5M=20)

1) Explain the IEEE single-precision format for Floating point number representation using a diagram.

2) Use the IEEE single- precision floating-point format for representing the value 1259.125

3) Write the Control Sequence for the execution of the instruction ADD R1, R2, R3 using the single bus organization.

4) Explain the connection and Control signals for the Memory Data Register (MDR) using a diagram.

Part B

Answer **all** the Questions. **Each** question carries **Twelve** marks. (5Qx12M=60)

5) i) Calculate the product of -13 and +6 Using Booth's Algorithm (6)
ii) Calculate the product of -13 and + 6 using Bit-pair recoding. (6)

6) i) Describe the disadvantage of an n- bit ripple carry adder.
ii) Explain how it is overcome in the case of a Carry look-ahead adder with a diagram
iii) State the equations for the various carry signals. (1+7+4)

7) i) Give the Control sequence for the ADD R4, R5, R6 instruction
ii) Explain how it is executed using a 3- bus organization
iii) Give the diagram for 3-bus organization (5+3+4)

8) Write the Restoring Division algorithm and use it to divide 8 by 3 using it. (5+7)

9) Write the Non-Restoring Division Algorithm and use it to divide 8 by 3. (5+7)