

Determine the physical address (or addresses) of the byte (or bytes) read or written in each of the instructions given below, and also Write the addressing mode for each instruction.

- a. ADD AX, [BX+8]
- c. ADD [BX+SI], CL

- b. MOV AL, [DI]
- d. MOV [BP+SI+10],AX

Part C

Answer the Question. Question carries **sixteen** marks.

(1Qx16M=16)

6. Write ALP program to

- a. Copy a block of data from one memory area to another memory area

(transfer 20 data from 40000H to 52000H), Use Register Indirect Addressing mode to read and write the data

- b. Add, Subtract, Multiply and divide 2 numbers 05h and 03h

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**PRESIDENCY UNIVERSITY
BENGALURU
SCHOOL OF ENGINEERING**

TEST - 2

Even Semester: 2018-19

Course Code: Microprocessor Programming and Interfacing

Course Name: ECE 207

Program & Sem: B.Tech & IV Sem

Date: 16 April 2019

Time: 1 Hour

Max Marks: 40

Weightage: 20%

Instructions:

- (i) Read the question properly and answer accordingly.
- (ii) Question paper consists of 3 parts.
- (iii) Scientific and Non-programmable calculators are permitted.

Part A

Answer **all** the Questions. **Each** Question carries **four** marks. (4Qx4M=16)

1. State the content of the register and the result obtained after the last instruction, all instructions executed sequentially. Assume that flags ZF, SF, CF, AF, OF, and PF are all initially reset.
MOV AL, 99H
MOV BL, 1BH
CMP AL, BL
2. Determine the new contents of AX and the flag register after executing the instruction: **SAR AX, CX**. If CX=02H and AX=091AH, assume that flags ZF, SF, CF, AF, OF, and PF are all initially reset.
3. Determine the new contents of AX and the flag register after executing the instructions: **ROL AX, CX**. If CX =01H and AX=1234H, assume that flags ZF, SF, CF, AF, OF, and PF are all initially reset.
4. Determine the new contents of AX and the flag register after executing the instruction: **XOR AX, 0098H**. If AX=3F0FH and assume that flags ZF, SF, CF, AF, OF, and PF are all initially reset

Part B

Answer the Question. The Question carries **eight** marks. (1Qx8M=8)

5. Explain the following instructions in detail :
(a) MOVSB/MOVSW (b) LODSB/LODSW (c) STOSB/STOSW
(d) SCASB/SCASW (e) CMPSB/CMPSW (f) REP
(g) REPE/REPZ (h) REPNE/REPZ

Part C

Answer the Question. The Question carries **sixteen** marks. (1Qx16M=16)

6. (a) Write an ALP to add the contents of registers AL, BL, CL and DL. Store the result of addition value to the memory location "SUM". The addition of numbers should be written inside the subroutine, use CALL and RET instruction.
(b) Write an ALP to add a data in one block of memory called "BLOCK1" with a data in another block of memory called "BLOCK2" using LOOP instruction. Data is 100 words. Store the result back in the same memory location, use string instructions.



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**PRESIDENCY UNIVERSITY
BENGALURU**

SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Even Semester: 2018-19

Course Code: ECE 207

Course Name: Microprocessor Programming and Interfacing

Program & Sem: B. Tech. & IV Sem

Date: 23 May 2019

Time: 3 Hours

Max Marks: 80

Weightage: 40%

Instructions:

- (i) Read the question properly and answer accordingly.
- (ii) Question paper consists of 3 parts.
- (iii) Scientific and Non-programmable calculators are permitted.

Part A

Answer **all** the Questions. **Each** question carries **two** marks.

(10Qx2M=20M)

i.	In an 8085 microprocessor if a number 56h is added with 77h, the status of CY and AC flags respectively will be: (a) 1, 1 (b) 0, 1 (c) 0, 0 (d) 1, 1
ii.	Among the available choices given below in an 8085 microprocessor the two externally initiated signals are (i) _____ and (ii) _____. HOLD, ALE, RD', WR' TRAP, CLK OUT
iii.	The 8086 can read a 16-bit word at an even address in (i) _____ operation and at an odd address in (ii) _____ operations. One, Two, Three, four, five
iv.	Among the internal registers listed below of 8086 microprocessor, (i) _____ register is a data register and (ii) _____ register is a segment register respectively. SP, CX, BP, SS, SI, DI
v.	In the Flag register of 8086 microprocessor, there are (i) _____ status flags and (ii) _____ control flags respectively. 5, 3, 6, 9, 8, 16
vi.	The addressing modes used in the following instruction CMP WORD PTR [BX+DI], 10 are (i) _____ + (ii) _____ respectively. BASE, RELATIVE, INDEX, REGISTER, IMMEDIATE, DIRECT
vii.	If two signed numbers 126d and 126d are added then the status of the (i) CY flag is _____ and (ii) OF flag is _____ respectively. (a) 1 and 0 (b) 0 and 1 (c) 1 and 1 (d) 0 and 0

viii.	The control word for setting the PC7 line of 8255 is (i) _____ and resetting the PC5 line of 8255 is (ii) _____ respectively. (a) AAh and ABh (b) F0h and FFh (c) 07h and 04h (d) 0Fh and 0Ah.
ix.	In an 8086 interrupt system if an INT 09 is executed, the memory location that will hold the corresponding Interrupt Service Routine (ISR) for (i) IP9 is _____ and for (ii) CS9 is _____ respectively in the interrupt vector table. (a) 00034h and 00037h (b) 00024h and 00026h (c) 00044h and 00046h (d) 00054h and 00057h
x.	The control word for configuring counter 2 of 8254 in mode 1 is (i) _____ and counter 1 of 8254 in mode 3 is (ii) _____ respectively. Counter 2 should be configured for binary count with LS Byte count, whereas counter 1 for BCD count with MS byte count. (a) 92h and 67h (b) 76h and 55h (c) 07h and 04h (d) 5Fh and 7Ah.

Part B

Answer **both** the Questions. **Each** question carries **ten** marks. (2Qx10M=20M)

2. What will be the final value in AX after executing the following instructions? Give the answer in both hexadecimal and binary. Indicate the AX, CL and CY values of each step as given in the table in hexadecimal.

mov al,15	AX=	CL=
mov ah,15	AX=	CL=
xor al,al	AX=	CL=
mov cl,3	AX=	CL=
shr ax,cl	AX=	CL=
add al,90h	AX=	CL= ; CY=
adc ah,0	AX=	

3. (a). Registers AX, BX, CX and DX contain the values 1111h, 2222h, 3333h and 4444h respectively. What are the contents of each register after the following sequence of instructions has executed?

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push ax
push cx
push bx
push dx
pop ax
pop bx
pop dx
pop cx

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- (b) How many times LOOP1 will be executed in the following program so that the contents of BL register becomes 21d? Show the value to be loaded in CL register.

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MOV BL, 00H
MOV CL, ??H
LOOP1: ADD BL, 03H
DEC CL
JNZ LOOP1

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Part C

Answer **both** the Questions. **Each** question carries **twenty** marks. (2Qx20M=40M)

4. Devise and develop the Memory Map and draw the Interfacing Diagram to interface a total of 20 KB memory using two 4Kx8 ROM and three 4Kx8 RAM Memory Chips with the 8088 microprocessor by indicating the necessary signals.

Note: Your Decoding logic should contain 74LS138 decoder and any suitable logic gate.

5. (a) The ports of an 8255 are connected in Simple I/O mode as: Port B – 8 LEDs (O/Ps), Port C Lower and Upper – 8 switches (I/Ps). Show (a) Control word to configure the 8255 as above (b) Addresses for all ports including the control register if the base (Port A) address is 60h and (c) Draw the required interfacing diagram.
- (b) In an 8254 device, Counter-1 is programmed for BCD counting with a count value of 55h in mode 3 (Square Wave Generator). Show (a) Control word to configure the 8254 (b) Addresses for all counters including the control register if the base (Counter-0) address is 41h and (c) Draw the required interfacing diagram.



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SCHOOL OF ENGINEERING

SUMMER TERM/ MAKE UP END TERM EXAMINATION

Semester: Summer Term 2019

Date: 26 July 2019

Course Code: ECE 207

Time: 2 Hours

Course Name: Microprocessor Programming and Interfacing

Max Marks: 80

Program & Sem: B. Tech. & IV Sem (2016 Batch)

Weightage: 40%

Instructions:

- (i) Read the question properly and answer accordingly.
- (ii) Question paper consists of 3 parts.
- (iii) Scientific and Non-programmable calculators are permitted.

Part A

Answer **both** the Questions. **Each** question carries **ten** marks. (2Qx10M=20M)

1. Differentiate between (a) Absolute Decoding and Partial Decoding (b) Differentiate between (a) Absolute Decoding and Partial Decoding (b) Fixed and Variable port addressing in terms of IN and OUT Instructions by giving examples.
2. Write the BSR control word by giving their hexadecimal values for resetting PC7, PC5, PC3 and setting PC6, PC4, PC2. Show each bits configured by you.

Part B

Answer **both** the Questions. **Each** question carries **fifteen** marks. (2Qx15M=30M)

3. The ports of an 8255 are connected in Simple I/O mode as: Port A – 8 LEDs (O/Ps), Port B – 8 switches (I/Ps). Show (a) control word to configure the 8255 as above (b) addresses for all ports including the control register if the base (Port A) address is 80h and (c) Draw the required interfacing diagram, and (d) the required program to complete the above task. (Assume that the delay is available.)
4. In an 8254 device, Counter-1 is programmed for binary counting with a count value of 44h in mode 3 (Square Wave Generator). Show (a) control word to configure the 8254 (b) addresses for all counters including the control register if the base (Counter-0) address is 60h and (c) Draw the required interfacing diagram, and (d) the required program to complete the above task.

Part C

Answer the **following** Question. **The** question carries **thirty** marks. (1Qx30M=30M)

5. Devise and develop the Memory Map and draw the Interfacing Diagram to interface a total of 64 KB memory using 8Kx8 ROM and 8Kx8 SRAM Memory Chips equal in number with the 8088 microprocessor by indicating the necessary signals.

Note: Your Decoding logic should contain 74LS138 decoder and any suitable logic gate.

