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GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST – 1

Even Semester: 2018-19 | **Date**: 01 March 2019

Course Code: ECE 215 / EEE 217 | **Time**: 1 Hour

Course Name: VLSI Design | **Max Marks**: 40

Programme & Sem: B. Tech. & VIII Sem (Group-I) | **Weightage**: 20%

Instructions:

(i) Read the question properly and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and Non-programmable calculators are permitted.

Part A

Answer **all** the Questions. **Each** question carries **four** marks. (4Qx4M=16)

1. Define the following SPICE parameters in not more than one sentence each: LAMBDA (λ) parameter, KP parameter, NSUB parameter and PHI parameter.
2. Calculate the MOS transistor gain factor (β) if the typical values for an nMOS process technology are given as below:
   Thickness of oxide = t_{ox} = 140 Å,
   $\epsilon = 3.9\ \epsilon_0$ => permittivity of SiO_2,
   Mobility of electrons = μ_n = 400 cm^2 / V-sec
3. Design a 2-input XNOR gate using Transmission Gates.
4. Define Noise Margin by plotting the input and output characteristics and voltage levels.

Part B

Answer the Question. Question carries **eight** marks. (1Qx8M=8)

5. Draw the VLSI Design Flow Chart which depicts the IC design steps.

Part C

Answer the Question. Question carries **sixteen** marks. (1Qx16M=16)

6. Draw the CMOS transistor network implementation of the Boolean expression:

$$F = \overline{DE + C(A + B)}$$

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TEST - 2

Even Semester: 2018-19 | **Date**: 13 April 2019

Course Code: ECE 215 / EEE 217 | **Time**: 1 Hour

Course Name: VLSI Design | **Max Marks**: 40

Program & Sem: B.Tech. & VIII Sem (Group-I) | **Weightage**: 20%

Instructions:

(i) Read the question properly and answer accordingly.

(ii) Question paper consists of 3 parts.

(iii) Scientific and Non-programmable calculators are permitted.

Part A

Answer **all** the Questions. **Each** question carries **five** marks. (3Qx5M=15)

1. Give a rough sketch (use pen only) of n-well manufacturing process by listing at least five important steps.
2. What do you mean by λ-based Layout Design Rules? Indicate the numerical values of λ in the Fig. Q2.
3. For the circuit shown in Fig. Q3, find the number of Euler's Paths possible and list each one of them.

Part B

Answer the Question. The question carries **nine** marks. (1Qx9M=9)

4. For a 6-input static OR gate (NOR3 + NAND2 logic) shown in Fig. Q4, each input can drive no more than 30λ of transistor width. The output must drive a 60/30 inverter (i.e., an inverter with a 60λ wide pMOS and 30λ wide nMOS transistor). Calculate (a) Branching effort (B), (b) Electrical effort (H), (c) Logical Effort (G), (d) Path Effort (F), (e) Best Stage Effort ($\hat{f}$) and (f) Minimum Path Delay (D).

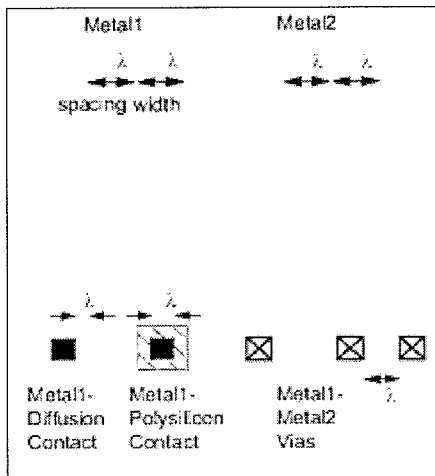

Fig. Q2

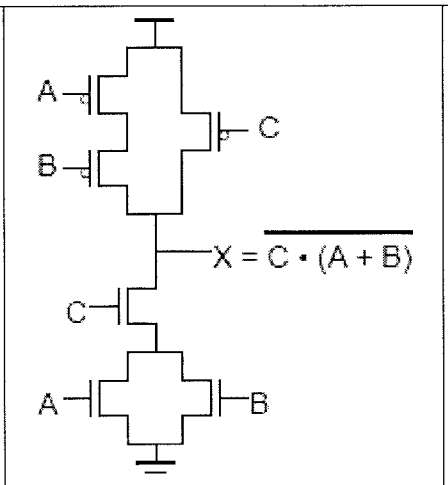

Fig. Q3

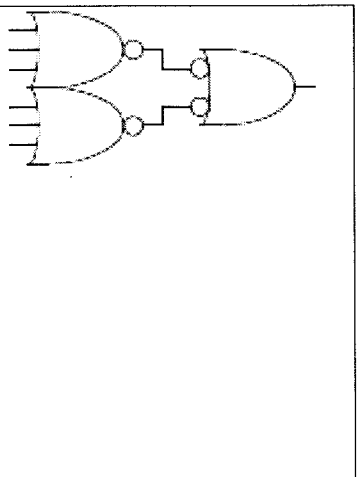

Fig. Q4

Part C

Answer the Question. The Question carries **sixteen** marks. (1Qx16M=16)

5. For the Boolean expression $Y = \overline{(A + B).C}$
   (a) Draw the CMOS transistor network implementation. (6 Marks)
   (b) Sketch a normal stick diagram. (10 Marks)

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SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Even Semester: 2018-19 | **Date**: 20 May 2019

Course Code: ECE 215 / EEE 217 | **Time**: 3 Hours

Course Name: VLSI Design | **Max Marks**: 80

Program & Sem: B.Tech & VIII Sem (Group-I) | **Weightage**: 40%

Instructions:

(i) Read the question properly and answer accordingly.

(ii) Question paper consists of 3 parts. For Part A, fill in the blanks from the given choices in proper order.

(iii) Scientific and Non-programmable calculators are permitted.

Part A

Answer **all** the Questions. **Each** question carries **two** marks. (10Qx2M=20M)

1	In 1965, Gordon Moore predicted that the number of transistors per chip would grow _____ i.e. double every _____ months. (exponentially, 14, linearly, 18, exponentially, annually)
2	VLSI chip manufacturers introduce a new process generation (also called a technology node) every 2–3 years with a _____ smaller feature size to pack _____ as many transistors in the same area respectively. (30%, twice, 40%, 35%, thrice, 50%)
3	The effect of channel-length modulation is less for a _____ MOSFET than for a _____ MOSFET respectively. (long-channel, short-channel, pMOS, nMOS, none of these)
4	In a MOS device the I_{ON} _____ with temperature whereas the I_{OFF} _____ with temperature respectively. (saturates, decreases, increases, vanishes, none of these)
5	A pMOS transistor passes a _____, and a _____respectively. (strong 0, weak 0, weak 1 strong 1)
6	For n-well CMOS process, the bulk of the PMOS is the _____, whereas the bulk of the NMOS is the _____ respectively. (n-well, p-well, substrate, drain, source)
7	Logical effort of 2-input NAND gate is _____, whereas for 2-input NOR is _____ respectively.

	(4/3, 5/3, 7/3, 6/3, 9/3)

8	Registers a, b are declared as **reg [2:0] a,b;**. a and b have initial values of 3 and 1 respectively . The values of a and b respectively are _____ and _____, after each of the following Verilog codes are executed.
	a = b + 2;
	b = a + 2;
	
	(1, 0, 3, 5. 2)

9	Which of the two following statements are true for Verilog modules? (a) A module can contain definitions of other modules. (b) When a module X is called multiple numbers of times from some other module, only one copy of module X is included in the hardware after synthesis. (c) More than one module can be instantiated within another module. (d) If a module X is instantiated 4 times within another module, 4 copies of X are created.
10	The current mirror circuits replicate current available at the _____ to the _____ respectively. (input, output, common terminal, none of these)

Part B

Answer the Question. The question carries **ten** marks. (1Qx20M=20M)

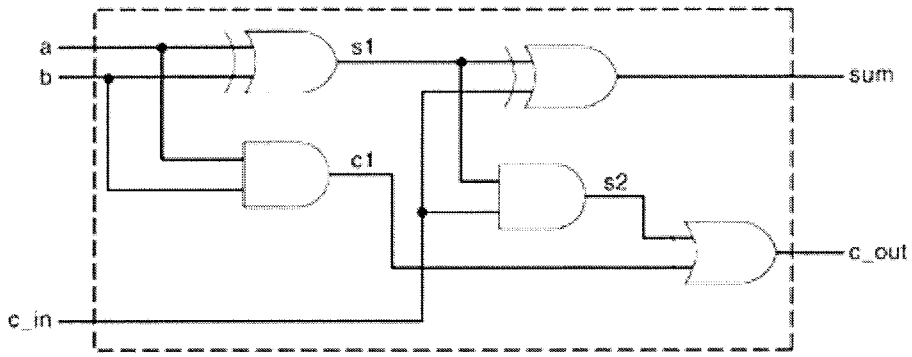
11. Consider the Boolean expression: $F = \overline{(A + B + C).(D + E)}$

(a) Draw the CMOS transistor network implementation.
(b) Sketch a normal stick diagram.
(c) Find the Euler's Paths possible and list at least four of them.

Part C

Answer **both** Questions. **Each** question carries **twenty** marks. (2Qx20M=40M)

12. Consider the circuit of a Full Adder shown below:



(a) Write the Structural Modeling Verilog code for the Full Adder.
(b) Draw the logic circuit diagram and write the Structural Modeling Verilog code for a 2-bit ripple carry adder by instantiating the Full Adder circuit in part (a). (20M)

13. (a) Draw the logic diagram of a 4:1 multiplexer which implements an XOR gate. Write the Verilog code for the circuit using behavioral modeling (use 'always' and 'case' statements). Given signals for the circuit are A and B as select lines and Z as output. (10M)
(b) Multiply two numbers 12 x -5 using Booth's Multiplication Algorithm and show each step in tabular format. (10M)