| Roll No. | | | | | | | | | | | | |
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**PRESIDENCY UNIVERSITY**
**BENGALURU**

**School of Engineering**

**Mid - Term Examinations - November 2024**

**Semester**: V | **Date**: 04/11/2024

**Course Code**: ECE3008 | **Time**: 09.30am to 11.00am

**Course Name**: VLSI Design | **Max Marks**: 50

**Program:** B.Tech | **Weightage**: 25%

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**Instructions:**

*(i) Read all questions carefully and answer accordingly.*

*(ii) Do not write anything on the question paper other than roll number.*

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**Part A**

**Answer ALL the Questions. Each question carries 2marks.** **5QX2M=10M**

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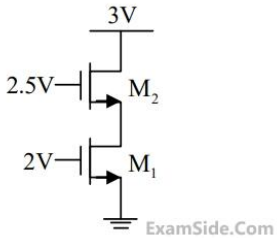
|---|---|---|---|---|
| **1** | What's the relationship between the drain and current in the MOSFET as a function of gate-to-source voltage and drain to source voltage? | 2 Marks | L1 | CO1 |
| **2** | Define MOS diode and mention at least two applications. | 2 Marks | L1 | CO1 |
| **3** | Define Substrate Bias effect. | 2 Marks | L1 | CO2 |
| **4** | The current conduction in the channel is in the form of drift. If the mobility falls at high temperatures, what can we say about the on-resistance as the temperature goes up? | 2 Marks | L1 | CO2 |
| **5** | Identify the region of operation of transistor M1 and M2 | 2 Marks | L1 | CO1,2 |




**Part B**

**Answer ALL Questions. Each question carries 10 marks.** **4QX10M=40M**

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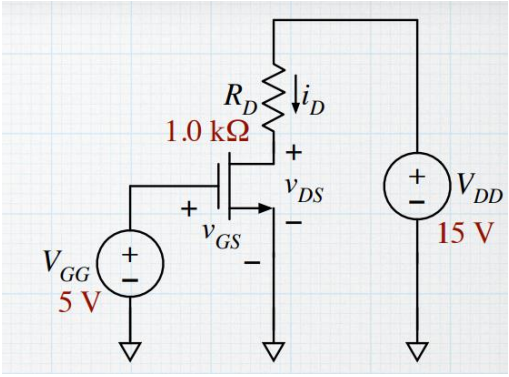
| **6** | **a.** | MOS transistor switches ON when a proper voltage is applied at the gate terminal. Calculate the current flow in the NMOS with | 6 Marks | L3 | CO1 |

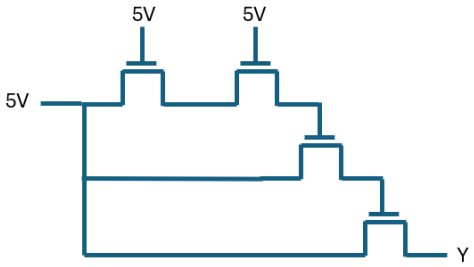
| | | | | | |
|---|---|---|---|---|---|
| | | the following parameters. L= 2μm. W =10 μm, $\mu_n$ = 0.05$m^2$/v-s, Cox = 1.5 ∗ $10^{-4}$ F/m2, VT = 0.4V.<br>i). VGS = 0.45v, VDS = 0 V<br>ii). VGS = 0.8 v, VDS = 0.4 V | | | |
| | **b.** | Identify the region of operation for each case. | 4 Marks | L1 | CO1 |
| | | or | | | |
| **7** | | The active load is used in n-MOSFET inverter to reduce the area of the chip. Derive small signal gain and output resistance of n-MOSFET inverter with active load. | 10 Marks | L3 | CO1 |
| **8** | **a.** | The metal oxide semiconductor transistor or MOS transistor is a basic building block in logic chips, processors & modern digital memories. Explain the operation for NMOS transistor in different regions (Cut-off, Linear and Saturation regions). | 6 Marks | L2 | CO1 |
| | **b.** | Plot the ID-VDS and ID-VGS characteristics for different values of VGS and VDS respectively. | 4 Marks | L2 | CO1 |
| | | **or** | | | |
| **9** | **a.** | NMOS transistors operate by creating an inversion layer in a p-type transistor body. Define channel length modulation? | 3 Marks | L1 | CO1 |
| | **b.** | The current flowing through an NMOS (n-channel metal-oxide-semiconductor) transistor can be described by the basic equation. Derive drain current equation assuming channel length modulation. | 7 Marks | L3 | CO1 |
| **10** | **a.** | Discuss small signal equivalent circuit model of MOSFET without considering the effect of channel length modulation modelled by output resistance. | 5 Marks | L2 | CO2 |
| | **b.** | Summarize important Design techniques you would follow when doing a Layout for Digital Circuits? | 5 Marks | L2 | CO2 |
| | | or | | | |
| **11** | **a.** | NMOS is like a regular switch - applying a voltage (like flipping the switch) turns it on, allowing current (like light) to flow. For the circuit shown, use the the NMOS equations to find ID and VDS. | 7 Marks | L3 | CO2 |




| | | | | |
|---|---|---|---|---|
| **b.** | Why is the substrate in NMOS connected to Ground and in PMOS to VDD? | 3 Marks | L2 | CO2 |

| | | | | |
|---|---|---|---|---|
| **a.** | Stick diagrams are a means of capturing topography and layer information using simple diagrams. Draw the transistor level schematic (CMOS) and stick diagram for 3 input NAND gate | 6 Marks | L2 | CO2 |
| **b.** | For the given circuit, if the threshold voltage of each transistor is 0.5V, then what is the output voltage at node Y. | 4 Marks | L2 | CO2 |

**12**




**or**

| | | | | |
|---|---|---|---|---|
| **a.** | Stick diagrams are used to represent VLSI layouts in an abstract way, showing the relative placements and connections between different layers like polysilicon, diffusion, and metal layers. Draw the transistor level schematic (CMOS) and stick diagram for 3 input NOR gate | 6 Marks | L2 | CO2 |
| **b.** | Find out the voltage at P, Q, R for given NMOS transistor. Assume Vt=1V. | 4 Marks | L2 | CO2 |

**13**