Roll No.													
----------	--	--	--	--	--	--	--	--	--	--	--	--	--



School of Engineering

Mid-Term Examination - November 2024

Semester: I **Date**: 04/11/2024

Course Code: ECE2007 **Time**: 09.30am to 11.00am

Course Name: Digital Design Max Marks: 50

Program: B. Tech CSE & allied **Weightage**: 25%

Instructions:

1

(i) Read all questions carefully and answer accordingly.

Answer ALL the Questions. Each question carries 2marks.

(ii) Do not write anything on the question paper other than roll number.

Write the Truth table and Boolean expression for the output of a NOR

Part A

	gate.				
2	Binary addition binary addition	2 Marks	L1	CO1	
3	State Idempote Identity Law in	2 Marks	L1	CO1	
4	What is the pur	2 Marks	L1	CO1	
5	Boolean Algebr systems. Compl	2 Marks	L1	CO1	
		D 4 D			
		Part B			
Ans	wer ALL Questic	part B ons. Each question carries 10 marks.	4QX1	0M=40	M
Ans	De Morg conjuncti	ons. Each question carries 10 marks. an's laws are two transformation rules that relate ons and disjunctions through negation. Explain and the the truth table any one De Morgans law for three	4QX1 5 Marks	0M=40 L2	OM CO1

5QX2M=10M

L1

CO1

2 Marks

or

	a.	Boolean algebra is applied in computer electronic circuits. These circuits perform Boolean operations and these are called logic circuits and logic gates. Implement all the basic gates using NOR gates.	5 Marks	L2	CO1			
7	b.	A bulb in a stair case has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switch irrespective of the state of the other switch. Construct the truth table and write the expression, identify the logic gate and also draw the logic symbol for the same.	5 Marks	L2	CO1			
8		You are designing a digital circuit that performs binary subtraction for a system that processes binary numbers. The system must subtract three binary bits. To achieve this, identify the logic circuit and design the system and implement the same using basic gates.	10 Marks	L3	CO2			
		or						
9		A comparator used to compare two binary numbers each of two bits is called a 2-bit magnitude comparator. Design a combinational circuit that compares two 2-bit binary numbers and implement the same using basic gates only for greater and less than conditions.	10 Marks	L3	CO2			
a.	a.	A K-map organizes truth table values into a grid format where adjacent cells differ by only one bit. Simplify the expression using K-map and mention the implicants and prime implicants for the same. $F(A,B,C,D)=\Sigma m(0,2,3,5,7,11,13,14,15)$.	5 Marks	L2	C01			
10	b.	Product of Sums (POS) is another form of Boolean expression where multiple sum terms (ORed variables) are multiplied together (ANDed). Convert the given function into minimal POS form $F(A,B,C) = \Pi M (0,1,3)$ and implement using basic gates.	5 Marks	L2	CO1			
or								
11	a.	In digital logic design, both SOP and POS forms have two main types:Canonical (or Standard) form and Non-Canonical (or Simplified) form.Convert the given expression into canonical SOP form. $Y = A'B + BC' + A'C$	5 Marks	L2	CO1			

	b.	K-map allows easy identification of common terms, leading to the simplification of logic expressions. Simplify the function given using k-map $Y = \Pi M (0,2,6,7,8,10,12,13)$	5 Marks	L2	CO1
12		The Half subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, the minuend and subtrahend and two outputs the difference and borrow out. Design half subtractor circuit and implement using basic gates. Also define combinational circuit.	10 Marks	L3	CO2
		or			
13		Half adder is a combinational arithmetic circuit that adds two inputs and produces an output of sum bit (s) and carry bit (c). Design half adder circuit and implement using NAND gates. And also list the steps to design the combinational circuits.	10 Marks	L3	CO2