Roll No.												

PRESIDENCY UNIVERSITY
BENGALURU

School of Engineering

Mid - Term Examinations - Nov 2024

Semester: VII | **Date**: 05/11/2024

Course Code: ECE3046 | **Time**: 02:00p m – 03:30pm

Course Name: Low Power VLSI Design | **Max Marks**: 50

Program: B. Tech- ECE | **Weightage**: 25%

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **5QX2M=10M**

1	The power dissipation reduction technique is applied from operating level to technology level. Mention three parts that the designer can perform low power technique to reduce power.	**2Marks**	**L1**	**CO1**
2	The Silicon on Insulator (SoI) technology supports various low power applications. List out the advantages of SoI.	**2Marks**	**L1**	**CO1**
3	In CMOS circuits, dynamic power is dissipated when energy is drawn from the power supply to charge up the output node capacitance. What are the different capacitances at the specified logic gate?	**2Marks**	**L1**	**CO1**
4	The channel length is reduced in short-channel devices to increase the number of transistors in IC. When are the devices referred to as short-channel devices?	**2Marks**	**L1**	**CO1**
5	SPICE (Simulation Program with integrated Circuit Emphasis) is a general-purpose analog circuit simulation. What are the differences between LTSPICE and HTSPICE?	**2Marks**	**L1**	**CO2**

Part B

Answer ALL Questions. Each question carries 10 marks. **4QX10M=40M**

6	The dynamic power dissipated during the nodes' charging and discharging of the CMOS logic circuit. Derive the expression for dynamic power dissipation.	**10Marks**	**L2**	**CO1**
	Or			
7	The short-circuit energy dissipation results due to a direct path current flowing from the power supply to the ground during the switching of a static CMOS gate. Derive the expression for short circuit power dissipation in CMOS inverter circuit.	**10Marks**	**L3**	**CO1**
8	Glitch power comes under dynamic dissipation in the circuit and is directly proportional to switching activity. Glitch power dissipation is 20%–70% of total power dissipation and hence glitching should be eliminated for low power circuits. (a) Explain glitch power dissipation with suitable example. (b) Illustrate GIBL.	**10Marks**	**L2**	**CO1**
	Or			
9	The VTCMOS is one of the methods to reduce leakage power. Describe VTCMOS.	**10Marks**	**L2**	**CO1**
10	The RC delay approximation is used to transistor sizing. The RC Delay Model helps in delay estimation CMOS circuit. Realize Y=(DE+(A*(B+C)))' and evaluate the sizing of the transistor.	**10Marks**	**L3**	**CO1**
	Or			
11	The sizing of the transistor is finding the (W/L) value of the MOS transistor. Realize Y=((A+B).(C+D).E)' and evaluate the sizing of the transistor.	**10Marks**	**L3**	**CO1**
12	Gate level logic simulation (GLS) is a reliable analysis in IC fabrication. Describe GLS.	**10Marks**	**L2**	**CO2**
	or			
13	Event-drive logic is one of the gate-level logic simulation techniques. Describe power components measured in event-driven logic simulation.	**10Marks**	**L2**	**CO2**