Roll No.												

PRESIDENCY UNIVERSITY
BENGALURU

School of Engineering

Mid - Term Examinations - Nov 2024

Semester: 5th | **Date**: 06/11/2024

Course Code: ECE3090 | **Time**: 02.00pm to 03.30pm

Course Name: Digital System Design using VERILOG | **Max Marks**: 50

Program:B.Tech | **Weightage**: 25%

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **2Mx5Q=10M**

1	VLSI is an implementation technology for electronic circuitry analogue or digital. List two popular VLSI platforms.	2 Marks	L1	CO1
2	Design methodology and hierarchy deiced the approach of solving the problems List two design methodology described in Verilog designing.	2 Marks	L1	CO1
3	Demonstrate the levels of abstraction in VLSI using necessary diagram.	2 Marks	L1	CO1
4	The basic unit of description in Verilog is the module, define module to design a X-Nor gate.	2 Marks	L1	CO1
5	Explain the types of delays in Gate Level modeling of Verilog HDL with examples	2 Marks	L1	CO2

Part B

Answer ALL Questions. Each question carries 10 marks. **4QX10M=40M**

6	**6a**	Develop the Verilog HDL code for the SR Flip Flop using the logic diagram. Verify the developed code by using suitable test the input cases.	4 Marks	L3	CO2
	6b	Utilize NAND gate to design the full adder circuit in gate level modeling of Verilog HDL code. Verify the developed code using the Test bench.	6 Marks	L3	CO2

OR

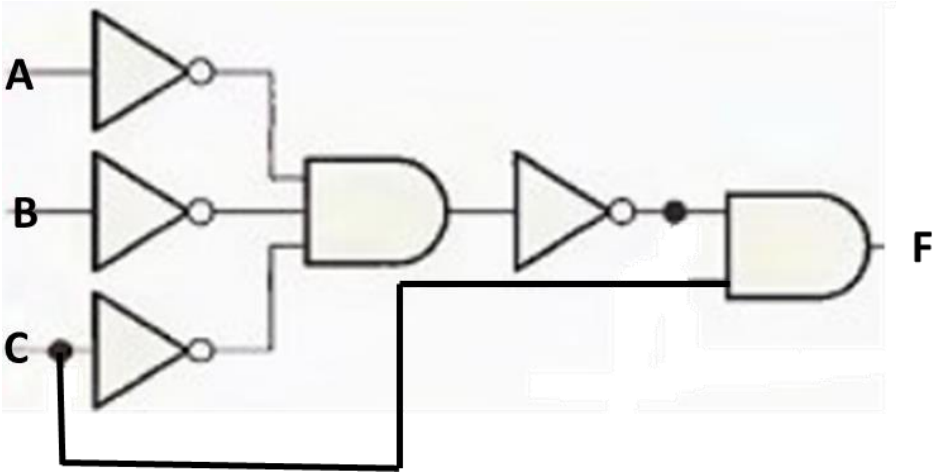
7	**7a**	Model the 3 input NAND gate in transistor level to verify using the test bench	4 Marks	L3	CO2
	7b	Make use of 2 input EXOR gate transistor level circuit to verify its truth table.	6 Marks	L3	CO2
8	**8a**	Model the 8:3 Encoder using the Boolean expression and verify the test cases of the input.	4 Marks	L3	CO1
	8b	Develop the ALU circuit with using the conditional operator with its test bench.	6 Marks	L3	CO1

OR

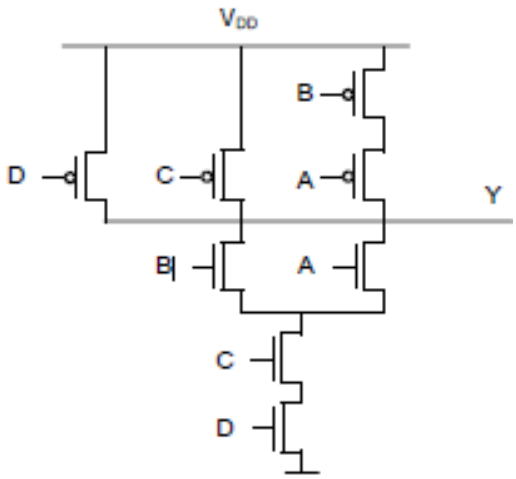
9	**9a**	Develop the D-Flip Flop using the Dataflow modeling and simulate for all the test cases.	4 Marks	L3	CO1
	9b	Utilize NOR gate to design the full subtractor in dataflow modeling of Verilog HDL code. Verify the developed code using the Test bench.	6 Marks	L3	CO1
10	**10a**	In data flow modelling the keyword "assign" is used to define the output of a circuit. Draw the schematic corresponding to the output equation given below which uses conditional operators: assign y = a ? (b ? i1 : i2) : (c ? i3 : i4)	6 Marks	L	CO1
	10b	Draw the schematic of the logic circuit described by the Verilog code below: module example (a, b, c, y); input a, b, c; output y; assign y = ~a & b & ~c | ~a & ~b & ~c | a & ~b & ~c; endmodule	4 Marks	L	CO2

OR

11	**11a**	A combinational circuit is a type of logic where each output depends only on its present input. For the combinational circuit shown below, write the Gate Level (Structural) Verilog description. Make sure that the internal and external signals are properly labeled.	6 Marks	L	CO2



	11b	Write the test bench for the circuit shown in 11(a) above.	4 Marks	L	CO2
12	**12a**	Switch level modeling in Verilog is a method used to describe digital circuits by focusing on the behavior of MOS transistors as electronic switches. For the circuit shown below, write the expression for the output 'Y' and write the Switch Level Verilog description. Make sure that the internal and external signals are properly labeled.	6 Marks	L	CO2



	12b	Write the test bench for the circuit shown in 12(a) above by considering only 4 combinations in which one of the transistors will have an input '1' and remaining three will have '0s'. e.g. ABCD = 1000.	4 Marks	L	CO2

OR

13	**13a**	Construct the 3 input NOR gate in transistor level modelling.	4 Marks	L	CO
	13b	Develop the function F = A +B(C+D) using the switch level modeling and verify using the test bench.	6 Marks	L	CO