Roll No.												

PRESIDENCY UNIVERSITY
BENGALURU

School of Engineering

Mid - Term Examinations - November 2024

Semester: III
Course Code: ECE2013
Course Name: Digital System Design using HDL
Program: B.Tech (VLSI)

Date: 06/11/2024
Time: 11.45am to 01.15pm
Max Marks: 50
Weightage: 25%

Instructions:

(i) Read all questions carefully and answer accordingly.
(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **5Qx2M=10M**

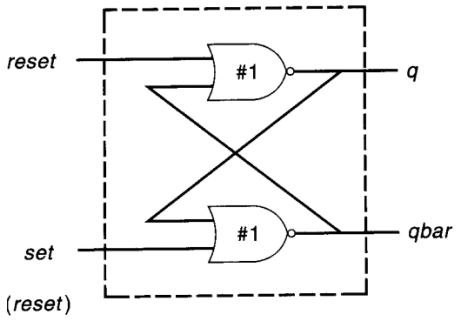
1	Operators perform some kind of operation on the operands. With a neat example explain the relational operators in Verilog	**2 Marks**	**L2**	**CO2**
2	Verilog contains the pre-defined system tasks and functions, including tasks for creating output from a simulation. What is the difference between the system tasks $monitor and $display	**2 Marks**	**L1**	**CO2**
3	Verilog supports a few compiler directives and system tasks what are compiler directives. Give 1 example.	**2 Marks**	**L1**	**CO1**
4	What is the Difference between a net and a register. How do you declare them in Verilog?	**2 Marks**	**L1**	**CO1**
5	In computer engineering, a hardware description language (HDL) is a specialized computer language used to describe the structure and behaviour of electronic circuits. Recall the differences between Verilog and VHDL	**2 Marks**	**L1**	**CO1**

Part B

Answer ALL Questions. Each question carries 10 marks. **4QX10M=40M**

6	**a.**	A JK flip-flop is a kind of sequential logic circuit that keeps track of binary data. Develop a Verilog code to implement JK flop using gate level modelling style	**4 Marks**	**L3**	**CO2**
	b.	A full subtractor is a combinational circuit that performs subtraction of two bits, one is minuend and other is subtrahend. Build a Full Subtractor using two half Subtractor in Verilog write the test bench code	**6 Marks**	**L3**	**CO2**

Or

7		 Fig. 1 set | reset | q_{n+1} 0 | 0 | q_n 0 | 1 | 0 1 | 0 | 1 1 | 1 | ? Fig. 2 The logic gate implementation is shown above in Fig 1. Develop Verilog description for RS latch. Include a delay of 1unit time when instantiating the NOR gate. Also write the stimulus(testbench) using the table show in Fig. 2 .	**10 Marks**	**L3**	**CO2**

8	**a.**	There are two basic types of sequence detectors: overlap and non-overlap. In a sequence detector that allows overlap, the final bits of one sequence can be the start of another sequence. Develop the state diagram of the Sequence detector to detect a sequence 00011 using No overlap method using both Mealy & Moore machine	**6Marks**	**L3**	**CO2**
	b.	An FSM is defined by a list of its states, its initial state, and the inputs that trigger each transition. Summarize the difference between Moore and mealy FSM	**4Marks**	**L1**	**CO2**

Or

9	**a.**	A Finite State Machine (FSM) is a mathematical model that is used to explain and understand the behavior of a digital system. Sequence detector is one such digital system. Develop the state	**6Marks**	**L3**	**CO2**

	diagram of a Sequence detector to detect a sequence 11011 using 1 bit overlap method using both mealy & Moore machine			
	b. If an input sequence of 11101101101110110 is given to the above Sequence detector determine the output in case of no overlap and 1 bit overlap	**4 Marks**	**L3**	**CO2**
10	One can determine whether incoming bits are equal to a prestored sequence by using a sequence detector. Build a Verilog code to implement the sequence detector in question 7a(i) and write the test bench code	**10 Marks**	**L3**	**CO2**
	Or			
11	A carry look-ahead adder reduces the propagation delay by introducing more complex hardware. Build a a Verilog code to implement a 4 bit Carry Look Ahead Adder using Verilog	**10 Marks**	**L3**	**CO2**
12	Verilog is a hardware description language used for simulation and synthesis in the field of computer science. Why Verilog is a popular HDL, Give reasons	**10 Marks**	**L1**	**CO1**
	Or			
13	Verilog is a hardware description language (HDL) used to model and design digital systems and circuits. Explain with examples the Modelling styles supported in Verilog.	**10 Marks**	**L2**	**CO1**