Roll No.											

PRESIDENCY UNIVERSITY

BENGALURU

School of Engineering

Mid - Term Examinations - November 2024

Semester: VII | **Date**: 05/11/2024

Course Code: ECE3050 | **Time**: 02:00pm – 03:30pm

Course Name: DESIGN FOR TESTABILITY | **Max Marks**: 50

Program: B. TECH | **Weightage**: 25%

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **5QX2M=10M**

1	What are the different types of fault classes?	**2 Marks**	**L1**	**CO1**
2	What are the DRCs that can result in low test coverage?	**2 Marks**	**L1**	**CO2**
3	To quantify of the ease of testing two terms are commonly used in DFT i.e controllable and Observable. Define what is controllability and Observability?	**2 Marks**	**L1**	**CO1**
4	Define the following terms. I) Defect ii) Fault	**2 Marks**	**L1**	**CO1**
5	What is the significance of Lock up latch in digital design testing?	**2 Marks**	**L1**	**CO2**

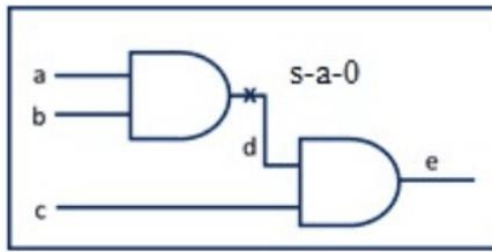
Part B

Answer ALL Questions. Each question carries 10 marks. **4QX10M=40M**

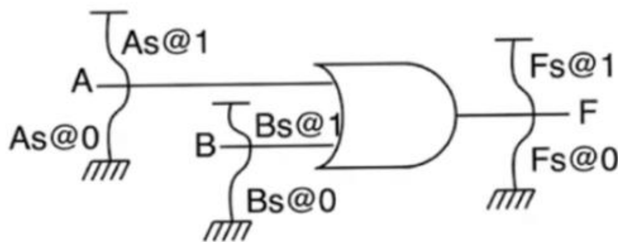
6	**6a.**	VLSI testing is important to designers, product engineers, test engineers, managers, manufacturers, and end-users. Discuss Testing during VLSI Lifecyle?	**5 Marks**	**L2**	**CO1**
	6b.	A VLSI design can be described at different levels of abstraction. Discuss different levels of abstraction in vlsi development process	**5 Marks**	**L2**	**CO1**

OR

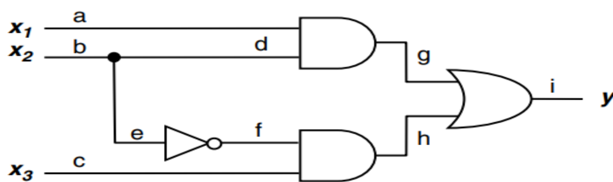
7	**7a.**	Find the test vector to be generated to detect stuck at 0 faults at net ‘d’ in the given circuit.	**5 Marks**	**L2**	**CO1**



	7b.	Find the test vector to be generated to detect faults at the input(A.B) and output(F) pf the OR gate which are stuck at 0 and 1 in the given circuit.	**5 Marks**	**L2**	**CO1**

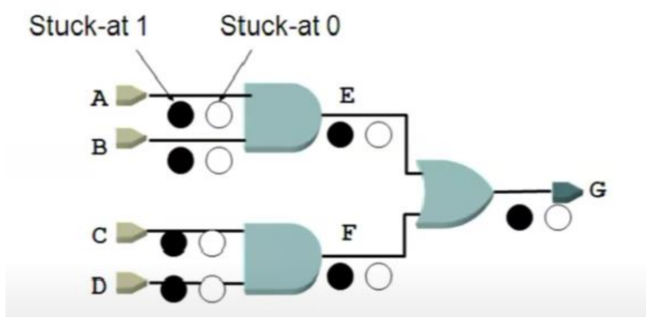


8		Design truth tables for the fault-free circuit and the faulty circuits for all possible single stuck-at faults.	**10Marks**	**L3**	**CO1**



OR

9		Design truth tables for the fault-free circuit and the faulty circuits for all possible single stuck-at faults.	**10Marks**	**L3**	**CO1**



Q.No		Question	Marks	Level	CO
10	**10a.**	In VLSI engineering a common fault after stuck at fault model is a bridging fault. Discuss the different types of bridging faults with an example.	**5 Marks**	**L3**	**CO2**
	10b.	IDDQ testing is a method for testing CMOS integrated circuits for the presence of manufacturing faults. Discuss Quiescent Drain Current testing(IDDQ)	**5 Marks**	**L3**	**CO2**
11	**11a.**	At the switch level, a transistor can be stuck-open or stuck-short, also referred to as stuck-off or stuck-on, respectively. Discuss Stuck-Open Fault Model with an example.	**5 Marks**	**L2**	**CO2**
	11b.	At the switch level, a transistor can be stuck-open or stuck-short, also referred to as stuck-off or stuck-on, respectively. Discuss Stuck-Short Fault Model with an example.	**5 Marks**	**L2**	**CO2**
12		Scan cell design is the most widely used structured DFT methodology. Explain about Edge triggered Muxed D Scan Cell design and test operation with suitable diagrams and waveforms?	**10Marks**	**L2**	**CO2**
		OR			
13		Within the field of electronics Level-sensitive scan design (LSSD) is part of an integrated circuit manufacturing test process. With neat diagram discuss the LSSD full scan design using double latch.	**10Marks**	**L2**	**CO2**