Roll No.												

PRESIDENCY UNIVERSITY
BENGALURU

School of Engineering

Mid - Term Examinations - November 2024

Semester: VII	**Date**: 05/11/2024
Course Code: ECE3050	**Time**: 11:45am – 01:15pm
Course Name: Design for Testability	**Max Marks**: 50
Program: B.Tech	**Weightage**: 25%

Instructions:

(i) Read all questions carefully and answer accordingly.
(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **2Mx5Q=10M**

1	What are the different types of fault classes?	2 Marks	L1	CO1
2	What are the DRCs that can result in low test coverage?	2 Marks	L1	CO2
3	Why we do IDDQ testing?	2 Marks	L1	CO2
4	What are the DRCs that can result in low test coverage?	2 Marks	L1	CO1
5	Define the following terms. i) Error ii) Fault	2 Marks	L1	CO1

Part B

Answer ALL Questions. Each question carries 10 marks. **4QX10M=40M**

6	Within the field of electronics Level-sensitive scan design (LSSD) is part of an integrated circuit manufacturing test process. With neat diagram discuss the LSSD full scan design using double latch.	10 Marks	L2	CO2
	OR			
7	Discuss advantages and disadvantages of three widely used scan cell designs: Muxed-D scan, clocked-scan, and level-sensitive scan design (LSSD)	10 Marks	L3	CO2

8	Scan cell design is the most widely used structured DFT methodology. Explain about a level-sensitive Scan Cell design and operation with suitable diagrams and waveforms?	10 Marks	L2	CO2
	OR			
9	LSSD is used for level-sensitive, latch-based designs with neat diagram discuss LSSD full scan cell design using polarity-hold shift register latch (SRL).	10 Marks	L3	CO2
10	There are different Scan architectures like full-scan design and partial scan design. Discuss Muxed D FULL Scan design architecture and operation with suitable waveforms?	10 Marks	L2	CO2
	OR			
11	There are different Scan architectures like full-scan design and partial scan design. Discuss Clocked FULL Scan design architecture and operation.	10 Marks	L2	CO2
12	In order to implement scan into a design, the design must comply with a set of scan design rules. With neat diagram discuss typical scan design rules and possible solution recommended for each scan design rule violation.	10 Marks	L3	CO2
	OR			
13	Design truth tables for the fault-free circuit and the faulty circuits for all possible single stuck-at faults.	10 Marks	L3	CO1