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 **PRESIDENCY UNIVERSITY**

  **Bengaluru**

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| **End - Term Examinations – JANUARY 2025** |
| **Date:** 03-01-2025 **Time:** 09:30 am – 12:30 pm |

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| **School:** SOE | **Program:** B.TECH ECE |
| **Course Code :** ECE3008 | **Course Name :** VLSI DESIGN |
| **Semester**: V | **Max Marks**: 100 | **Weightage**: 50% |

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| **CO - Levels** | **CO1** | **CO2** | **CO3** | **CO4** |
| **Marks** | **10** | **10** | **40** | **40** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Do not write anything on the question paper other than roll number.*

**Part A**

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| **Answer ALL the Questions. 10Q x 2 Marks=20 Marks** |
| **1** | N-channel MOSFET has a threshold voltage of 0.4V. In the saturation region at one point ID=2.25uA when VGS=0.5V. What will be the value of ID if VGS reaches to 0.7 V while operated in saturation region. | **2 Marks** | **L1** | **CO1** |
| **2** | Mention the operating conditions for 3 different regions of operation for NMOS transistor. | **2 Marks** | **L1** | **CO1** |
| **3** | For a MOSFET operating in saturation, how do gm and VGS-VTH change if both W=L and ID are halved? | **2 Marks** | **L1** | **CO2** |
| **4** | Define MOS diode and mention at least two application. | **2 Marks** | **L1** | **CO2** |
| **5** | State the factors that affects the output voltage swing for differential amplifier. | **2 Marks** | **L1** | **CO1** |
| **6** | Draw the CMOS schematic for given Boolean function: F=[(A+B)’.C’]’ | **2 Marks** | **L1**  | **CO1** |
| **7** | Draw the CMOS current mirror circuit using preferred equation. | **2 Marks** | **L1** | **CO2** |
| **8** | What are the different types of load configurations in Cascode amplifier. | **2 Marks** | **L1** | **CO2** |
| **9** | Draw CMOS Inverter using active load. | **2 Marks** | **L1** | **CO1** |
| **10** | What are the different types of load configurations in Cascode amplifier. | **2 Marks** | **L1** | **CO2** |

**Part B**

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| **Answer the Questions Total 80 Marks.** |
| **11.** | **a.** | Integrated chips are the building blocks of modern electronic systems, providing functionality and processing power in a compact and efficient package. Explain the ASIC Design flow process. | **10 Marks** | **sL2** | **CO4** |
|  | **b.** | Explain the difference between bad and good system partitioning using required examples. | **10 Marks** | **L2** | **CO4** |
| **Or** |
| **12.** | **a.** | Explain working of NMOS transistor using required diagram and cases. | **10 Marks** | **L2** | **CO4** |
|  | **b.** | Find the drain current and voltage at Q2. Assume λ=0.µnCox=200uA/$V^{2}$, Vt=0.6V and Id=80uA. | **10 Marks** | **L3** | **CO4** |
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| **13.** | **a.** | For the common-source amplifier of Fig, calculate the small-signal voltage gain and the bias values of Vi, and Vo at the edge of the triode region. Also calculate the bias values of Vi, and Vo where the small-signal voltage gain is unity with the transistor operating in the active region. What is the maximum voltage gain of this stage? Assume VDD=3V, RD=5KOhm, unCox =200uA/V2, W=10um, L=1 um, Vt = 0.6V, and lambda = 0. | **10 Marks** | **L3** | **CO3** |
|  | **b.** | Explain the working principle of Fully Differential amplifier using various cases. | **10 Marks** | **L3** | **CO3** |
| **Or** |
| **14.** | **a.** | Analyze the Cascode amplifier using PMOS current source with the help of small signal model. | **10 Marks** | **L3** | **CO3** |
|  | **b.** | Summarize the advantages of using High Gain Op-amp compared to single stage Op-amp. | **10 Marks** | **L2** | **CO3** |

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| **15.** | **a.** | A MOSFET in saturation drain current of 1 mA for VDS 0.5 volt and the channel length modulation coefficient is given 0.05 $V^{-1}$. Calculate the output resistance of the MOSFET. | **10 Marks** | **L2** | **CO3** |
|  | **b.** | If the NMOS device has µnCox=100uA/$V^{2}$, W=10um, L=1um, Vs=0V, Vt=0.7V. Find the drain current in all 3 cases given below:1. VD=0.5V
2. VD=0.9V
3. VD=3V
 | **10 Marks** | **L2** | **CO3** |
| **Or** |
| **16.** | **a.** | An NMOS transistor operating in the linear region has the drain current of 5 mA at VDS of 0.1 V. By keeping VGS constant VDS is increased to 1.5 V. Given µnCoxW/L=50uA/$V^{2}$. Calculate the trans conductance at new point. | **10 Marks** | **L2** | **CO3** |
|  | **b.** | Mention different regions of Operation for NMOS transistor using ID-VDS and ID-VGS graph and required equations. | **10 Marks** | **L2** | **CO3** |

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| **17.** | **a.** | For the closed loop amplifier circuit shown below, the magnitude of the open loop low frequency small signal voltage gain is 40dB. All the transistors are biased in saturation. The current bias is ideal. Neglect Body effect, channel length modulation and device capacitances. Calculate closed loop low frequency small signal voltage gain. | **10 Marks** | **L2** | **CO4** |
|  | **b.** | Design a fully differential amplifier with the specified gain of 9V, and input voltages Vin1= 1V and Vin2​=1V, we need to go through the following steps:Key Specifications are1. Differential Amplifier Gain = 9V (which is the differential voltage gain)
2. Vin1=Vin2=1V (input voltages)
3. The desired gain will be the difference between the output voltage at the positive and negative inputs.
4. Ibias=500uA
 | **10 Marks** | **L3** | **CO4** |
| **Or** |  |  | **10 Marks** | **L2** | **CO2** |
| **18.** | **a.** | An amplifier is used to increase the amplitude of a signal waveform, without changing other parameters of the waveform such as frequency or wave shape. Explain Common Source amplifier using a neat circuit diagram. | **10 Marks** | **L2** | **CO4** |
|  | **b.** | Analyze the small signal gain and the output resistance using preferred model for the above mentioned circuit. | **10 Marks** | **L3** | **CO4** |

**\*\*\*\*\* BEST WISHES \*\*\*\*\***