Roll No.												

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST 1

Sem & AY: Odd Sem 2019-20 | **Date**: 30.09.2019

Course Code: ECE 101 | **Time**: 1.00 PM to 2.00 PM

Course Name: ELEMENTS OF ELECTRONICS ENGINEERING | **Max Marks**: 30

Program & Sem: B.Tech (Chemistry Cycle) & I | **Weightage**: 15%

Instructions:

(i) Read Questions carefully and answer accordingly
(ii) Scientific and Non- programmable calculators are permitted
(iii) This question paper contains two pages

Part A [Memory Recall Questions]

Answer all the Questions. Each Question carries one mark. (10Qx1M=10M)

1. Choose the correct answer (i-x)(C.O.NO.1) [Knowledge]

i. While performing an experiment in Basic Electronics lab, two students got a resistor R_1. If the value of R_1 is 16KΩ then determine colour bands of R_1
(a) R_1: $Brown\ Blue\ Orange$
(b) R_1: $Brown\ Green\ Red$
(c) R_1: $Black\ Brown\ Red$
(d) Cannot be determined

ii. Two resistors R1 of 20Ω and R2 of 40Ω are connected in parallel, the equivalent resistance of the circuit is:
(a) 13.33Ω (b) 133.3Ω (c) 1.33Ω (d) 18Ω

iii. Name the law which relates voltage in a device with its current:
(a) Kirchoff's current law, $I_1 + I_2 - I_3 = 0$
(b) Kirchoff's voltage law, $V - V_1 - V_2 = 0$
(c) Ohm's law, R=VI
(d) Ohm's law, V=IR

iv. N-type semiconductor is formed by doping pure Silicon or Germanium with impurity atoms that are:
(a) Trivalent (b) Pentavalent (c) Both (d) None of these

v. In P-type semiconductor material, majority charge carriers are:
(a) Electrons (b) Holes (c) Both Electrons and Holes (d) None of these

vi. Conductors, semiconductors and insulators can be classified using Energy bands. At 0K, semiconductor behaves as:
(a) Conductor
(b) Insulator
(c) Semiconductor
(d) Metal

vii. For an ideal PN junction diode, which of the following analogy is true:
(a) Forward Biased::R=0 (b) Forward Biased::R→∞ (c) Reverse Biased::R=0
(d) None of these

viii. In Shockley's Equation, the thermal voltage V_T is determined by:
(a) $T/11{,}800$
(b) T/kq
(c) $T/11{,}600$
(d) Cannot be determined

ix. RMS output voltage of full-wave rectifier is:
(a) $V_{rms} = V_m/\sqrt{2}$ (b) $V_{rms} = V_m/\pi$ (c) $V_{rms} = V_m/2$ (d) None of these

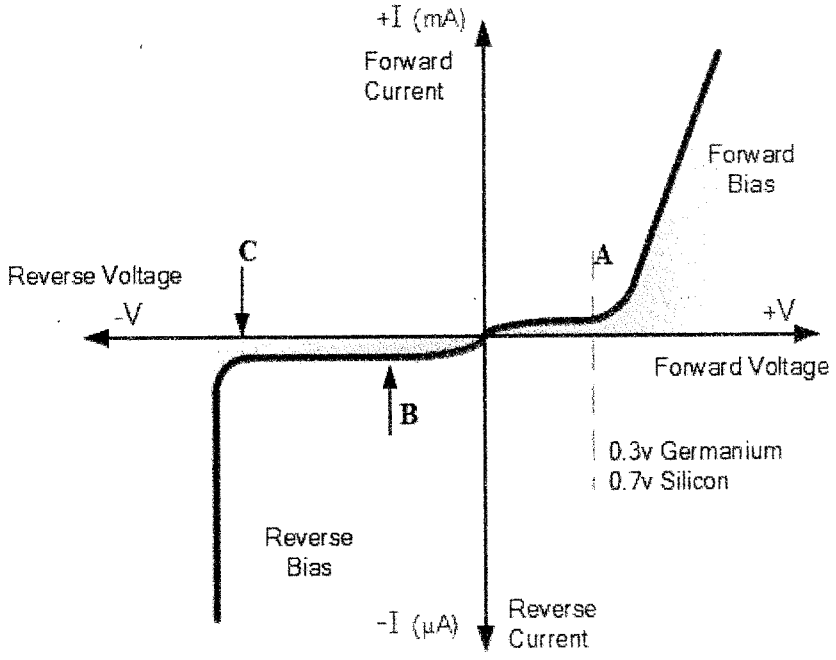
x. Ripple Factor of a full-wave rectifier is:
(a) 1.21 (b) 1.414 (c) 0.483 (d) 0.982

Part B [Thought Provoking Questions]

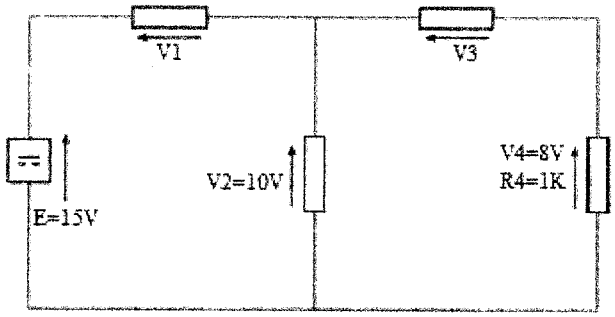
Answer both the Questions. Each Question carries five marks. **(2Qx5M=10M)**

(C.O.NO.1) [Comprehension]

2. The figure below represents PN junction diode characteristics. Refer the figure and answer the following question. Identify point A, B and C and define each of them. Differentiate between static resistance and dynamic resistance.



3. For the given circuit, Identify and state the laws to be used to determine the values of V1, V3 and I4. Determine the values of V1, V3 and I4.



Part C [Problem Solving Questions]

Answer both the Questions. Each Question carries five marks. (2Qx5M=10M)

(Q4&Q5)(C.O.NO.1) [Comprehension]

4. Read the passage and answer the following question:
Extrinsic semiconductor materials are made by adding impurity called Dopant. This process of adding impurity is called Doping. Extrinsic semiconductor are of two types: P-type and N-type. P-type and N-type joined together form a P-N junction. The working of PN junction has three stages: No Bias, Forward Bias and Reverse Bias condition.

   i. Explain the working of P-N junction diode in forward bias condition with suitable diagram. [2M]

   ii. In a circuit, if supply voltage is 5V and load resistance is 100Ω and there is a silicon diode,determine the D.C. Loadline points and plot it. [3M]

5. Read the passage and answer the following questions:
Rectification is the process of converting A.C. components into D.C components. Rectifier is a device that converts A.C. voltage into pulsating D.C. voltage. Rectifiers can be classified into three types: Half-wave rectifier, Full-wave rectifier and Bridge rectifier.

   i. Write short note on half-wave rectifier with suitable diagrams. [3M]

   ii. Derive an expression of V_{odc} for half-wave rectifier [2M]

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

Even Semester: 2019-20
Course Code: ECE 101
Course Name: Elements of Electronics Engineering
Programme & Sem: BTech & 1st semester (Chemistry cycle)

Date: 30 September 2019
Time: 1 Hour
Max Marks: 30
Weightage: 15%

Extract of question distribution [outcome wise & level wise]

Q.NO.	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [10 Marks] Bloom's Levels	Thought provoking type [10Marks] Bloom's Levels	Problem Solving type [10 Marks]	Total Marks [30]
		Module - 1	K	C	C	
1-10	C.O.1	Module – 1 (10-Objective Type Questions)	10			10
1-2	C.O.1	Module – 1 (Subjective Type Questions)		5 5		10
1-2	C.O.1	Module – 1 (Subjective Type Questions)			5 5	10

	Total Marks			10			10			10		30

K =Knowledge Level C = Comprehension Level, A = Application Leve

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

[I hereby certify that All the questions are set as per the above guide lines. Ms. Trisha]

Reviewers' Comments (1) B. Tech (2) Q. Numbering should be re-done (3) Part C Q1- 5M but Scheme 6M (4) QP→Q2 Marks → End (Edit).

Annexure- II: Format of Answer Scheme

GAIN MORE KNOWLEDGE REACH GREATER HEIGHTS

SCHOOL OF ENGINEERING

SOLUTION

Semester: 1st
Course Code:ECE 101
Course Name: Elements of Electronic Engineering

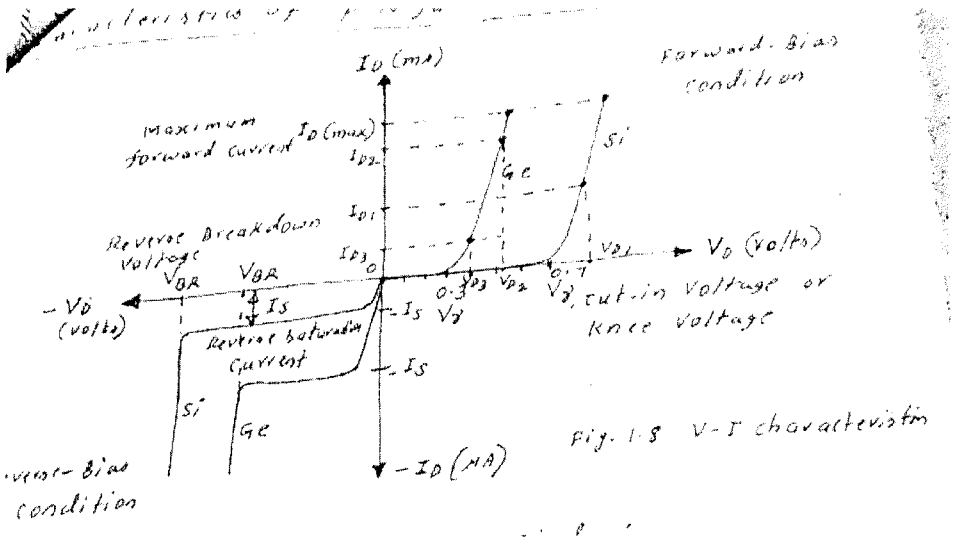
Date: 30-09-2019
Time: 1:00 PM – 2:00 PM
Max Marks: 30 Marks
Weightage: 15%

Part A (10Q x 1M = 10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1.	(a) R_1: *Brown Blue Orange*	1 M	1 min
2.	(a) 13.33Ω	1 M	1 min
3.	(d) Ohm's law, V=IR	1 M	1 min

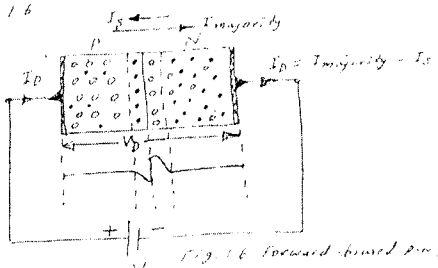
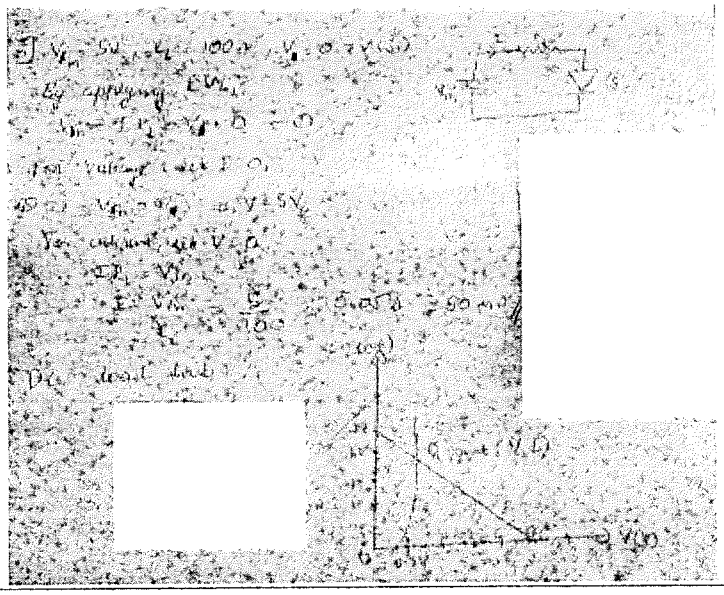
4.	(b) Pentavalent	1 M	**1 min**
5.	(b) Holes	1 M	**1 min**
6.	(b) Insulator	1 M	**1 min**
7.	(a) Forward Biased::R=0	1 M	**1 min**
8.	(c) $T/11{,}600$	1 M	**1 min**
9.	(a) $V_{rms} = V_m/\sqrt{2}$	1 M	**1 min**
10.	(c) 0.483	1 M	**1 min**

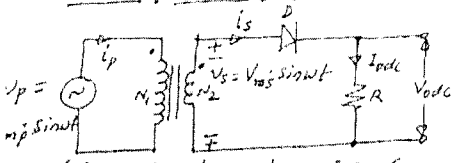
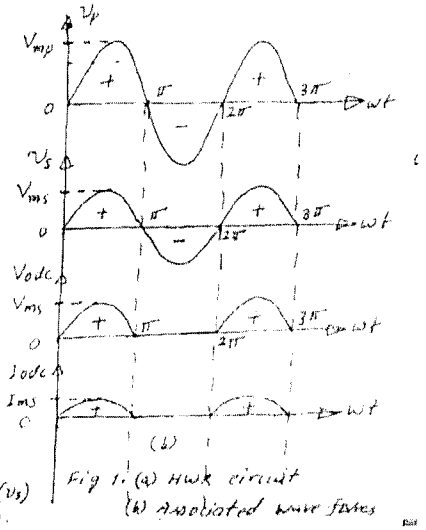
Part B **(2Q x 5M = 10 Marks)**

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1.	 Fig. 1.8 V-I characteristics A→Knee Voltage/cut-in voltage B→ Is: Reverse saturation current C→ Vbr: Breakdown voltage	Identify: - 0.5M each Definition 1M each Difference- 0.5M	10 Mins

	parameters of p-n junction diode 1. Cut-in voltage : Knee voltage (V_γ) It is the voltage at which diode current increases linearly. The cut-in voltage for Si diode is 0.7V and for Ge diode it is 0.3V. 5 Static resistance : dc resistance It is the ratio of fixed voltage and the corresponding fixed current both in forward and reverse bias condition. $R_S = \frac{V_{D1}}{I_{D1}} = \frac{-V_{D1}}{-I_{S1}}$ 6. Reverse Saturation Current : I_S It is the current due to minority carriers flows in reverse direction when the diode is under reverse-bias condition. 7. Reverse Breakdown Voltage : V_{BR} It is the reverse voltage at which junction breaks down and reverse current flows through the diode when it is under reverse-bias condition. 4. Dynamic resistance : ac resistance. ie It is the ratio of change in forward voltage to the change in forward current $r_d = \frac{\Delta V_D}{\Delta I_D}$		
2.	KVL and Ohm's Law: definition/expression V1=5V V3=2V I4=8mA	Identify & define: 1M each= 2M 3M	10 Mins

Part C (2Q x 5M = 10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1. i)	Forward-Bias Condition : A forward-bias condition is established by applying the positive potential to the p-type material and the negative potential to the N-type material as shown in figure 1.6  Fig 1.6 forward biased pn junction due to the application of forward bias, the holes in the p-type are repelled by the positive terminal of the bias	Diagram: 1M Explanation 2 M	
	are forced to move towards the junction (8) similarly the electrons in the N-type are repelled by the negative terminal of the bias and are forced to move towards the junction. consequently the width of the depletion region decreases. As a result current due to majority carriers flows from anode to cathode. The current due to minority carriers flows opposite to the majority current. Hence the diode current I_D is given by $I_D = I_{majority} - I_S$ As the applied voltage increases in magnitude, the depletion region will continue to decrease in width until a flood of electrons can pass through the junction		10 Mins
ii)		1M+1M+1M	

2. i)	I Half wave Rectifier :  (a) step down transformer  Fig 1: (a) HWR circuit (b) Associated wave forms Half wave rectifier circuit comprises of a step down transformer, a diode and a load resistor. In step down transformer the number of turns in primary winding (N_1) is more than the number of turns in the secondary winding (N_2). Hence secondary voltage (V_s) is less than the primary voltage (V_p). During positive half-cycle of the input a.c voltage, the diode D is forward-biased and conducts. Hence positive half cycle is dropped across load resistor R. During negative half-cycle of the input ac voltage, the diode D is reverse-biased and do not conducts. Hence there is no voltage drop across load resistor R. In HWR the load current can flow only during positive half-cycle and hence the name Half wave Rectifier.	1M+1M+1M	10 Mins
ii)	* Average output voltage and current : V_{dc}, I_{dc} The average output voltage for the waveform shown in Fig 1.(b) is given by $V_{dc} = \frac{1}{2\pi}\left[\int_0^{\pi} V_{ms}\sin\omega t\, d\omega t + \int_{\pi}^{2\pi} 0\, d\omega t\right]$ $V_{dc} = \frac{1}{2\pi}\int_0^{\pi} V_{ms}\sin\omega t\, d\omega t \longrightarrow (1)$ $= \frac{V_{ms}}{2\pi}\left\{-\cos\omega t\right\}_0^{\pi}$ $= \frac{V_{ms}}{2\pi}\left\{\cos 0 - \cos\pi\right\}$ $= \frac{V_{ms}}{2\pi}\left\{2\right\}$ $V_{dc} = \frac{V_{ms}}{\pi} = \frac{V_m}{\pi}$ Similarly $I_{dc} = \frac{I_{ms}}{\pi} = \frac{I_m}{\pi} \longrightarrow (2)$	2M	

Roll No.												

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST – 2

Sem & AY: Odd Sem 2019-20 | **Date:** 18.11.2019

Course Code: ECE 101 | **Time:** 1.00 PM to 2.00 PM

Course Name: ELEMENTS OF ELECTRONICS ENGINEERING | **Max Marks:** 30

Program & Sem: B. Tech (Chemistry Cycle) & I | **Weightage:** 15%

Instructions:

(i) ***Read the question properly and answer accordingly***

Part A [Memory Recall Questions]

Answer all the Question. Each Question carries one mark. (10x1M=10M)

(C.O.1 / C.O.2) [Comprehension Level]

1. A Full wave Bridge Rectifier uses
   (a) 2 Diodes and Step Down Transformer
   (b) 4 Diodes and Step Down Transformer
   (c) 2 Diodes and Center-Tapped Transformer
   (d) 4 Diodes and Center-Tapped Transformer
2. Filter is a circuit used to
   (a) remove the DC-Components present in the rectifier output
   (b) remove the AC-Ripples and DC Components present in the rectifier output
   (c) remove the AC-Ripple Components present in the rectifier output
   (d) None of the above
3. For a Half wave rectifier with capacitor filter the relationship between charging time T_1 , discharging time T_2 and the total Time T is given by:
   a. $T_2 >> T_1$ hence $T_2 = T$
   b. $T_2 << T_1$ hence $T_2 = T/2$
   c. $T_2 = T_1$ hence $T_2 = T$
   d. $T_2 = T_1$ hence $T_2 = T/2$
4. The Zener Diodes are special purpose diodes manufactured
   a. with Heavily doped Semiconductor to maintain Constant Current Level
   b. with Lightly doped Semiconductor to maintain Constant Voltage Level
   c. with Lightly doped Semiconductor to maintain Constant Current Level
   d. with Heavily doped Semiconductor to maintain Constant Voltage Level

5. In Bipolar Junction Transistor, the Terminals: Emitter - Base – Collector
   a. Heavily – Moderately – Lightly Doped
   b. Heavily – Lightly- Moderately Doped
   c. Moderately – Lightly- Heavily Doped
   d. Lightly – Moderately- Heavily Doped
6. For a NPN / PNP transistor to be operated in ACTIVE REGION the:
   a. Emitter-Base Junction is Reversed Biased and Collector-Base Junction is Forward Biased
   b. Emitter-Base Junction is Forward Biased and Collector-Base Junction is Reverse Biased
   c. Emitter-Base Junction is Reversed Biased and Collection-Base Junction is Reverse Biased
   d. Emitter-Base Junction is Forward Biased and Collection-Base Junction is Forward Biased
7. For a BJT the Current equation is :
   a. $I_E = I_C + I_B$
   b. $I_C = I_E + I_B$
   c. $I_B = I_C + I_E$
   d. $I_E = I_C - I_B$
8. The Relationship between β and α is
   a. $\beta = \frac{1}{1-\alpha}$
   b. $\beta = \frac{\alpha}{1+\alpha}$
   c. $\beta = \frac{\alpha}{1-\alpha}$
   d. $\beta = \frac{1-\alpha}{1+\alpha}$
9. The BJT is used as a switch when the Operating Point is in
   a. Cut-Off Region :: OFF STATE and Saturation Region :: ON STATE
   b. Saturation Region::OFF STATE and Cut-Off Region:: ON STATE
   c. Active Region:: OFF STATE and Saturation Region :: ON STATE
   d. Saturation Region::OFF STATE and Active Region :: ON STATE
10. For a BJT in Common Emitter Configuration the Current Gain is defined as:
   a. $\beta = \frac{IC}{IB}$
   b. $\beta = \frac{IB}{IE}$
   c. $\beta = \frac{IB}{IC}$
   d. $\beta = \frac{IC}{IE}$

(C.O.1 / C.O.2) [Comprehension Level]

Part B [Thought Provoking Questions]

Answer both the Questions. Each Question carries five marks. (2Qx5M=10M)

11. **Fill in the Blanks.** (C.O.1/ C.O.2) [Comprehension level]

a) The Avalanche Breakdown is caused due to high Kinetic Energy whereas Zener breakdown is due to high ----------.

b) If the base current is 100μA and current amplification factor is 100, then the collector current is ----------.

c) The relationship between the current gains α & β as $\alpha = \frac{\beta}{1+\beta}$ is True or False ? -------

d) "FIXED BIAS" transistor biasing circuit is also known as "BASE BIAS" circuit. True or False ? ----------

e) For a Silicon Transistor, operated in Common Emitter Configuration (CE), the Knee voltage across the Base-Emitter Terminals (V_{BE}) is ----------.

12.Explain with neat diagram the construction & working Principle of PNP or NPN Transistor. (C.O.2) [Comprehension level]

Part C [Problem Solving Questions]

Answer both the Questions. Each Question carries five marks. (2Qx5M=10M)

13. Sketch the V-I characteristics of a BJT in Common-Base and Common-Emitter Configuration with suitable Circuit diagram. (C.O.2) [Comprehension level]

14. For a Fixed Bias Circuit in CE configuration, with V_{cc}=30V, R_B=1.5MΩ, R_c=5KΩ, $\beta = 100$, neglecting V_{BE}, Draw the D-C Load Line and mark all the required quantities in the plot. (C.O.2) [Comprehension level]

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

Semester: 1st
Course Code: ECE 101
Course Name: Elements of Electronic Engineering

Date: 18-11-2019
Time: 1:00 PM – 2:00 PM
Max Marks:30 Marks
Weightage: 15%

Extract of question distribution [outcome wise & level wise]

Q.NO	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [10 Marks] Bloom's Levels			Thought provoking type [10Marks] Bloom's Levels			Problem Solving type [10 Marks]			Total Marks [30]
		Module – 1,2	C			C			C			
1-10	C.O.1/ C.O.2	Module – 1 M0dule-2 (10-Objective Type Questions)	10									10
1-2	C.O.1/ C.O.2	Module –1 Module - 2 (Subjective Type Questions)				5	5					10
1-2	C.O.2	Module – 2 (Subjective Type Questions)							5	5		10

	Total Marks			10			10			10		30

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

Annexure- II: Format of Answer Scheme

GAIN MORE KNOWLEDGE REACH GREATER HEIGHTS

SCHOOL OF ENGINEERING

SOLUTION

Semester: 1st

Course Code:ECE 101

Course Name: Elements of Electronic Engineering

Date: 18-11-2019

Time: 1:00 PM – 2:00 PM

Max Marks: 30 Marks

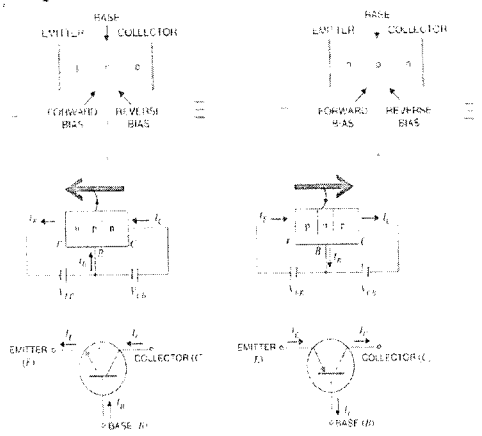
Weightage: 15%

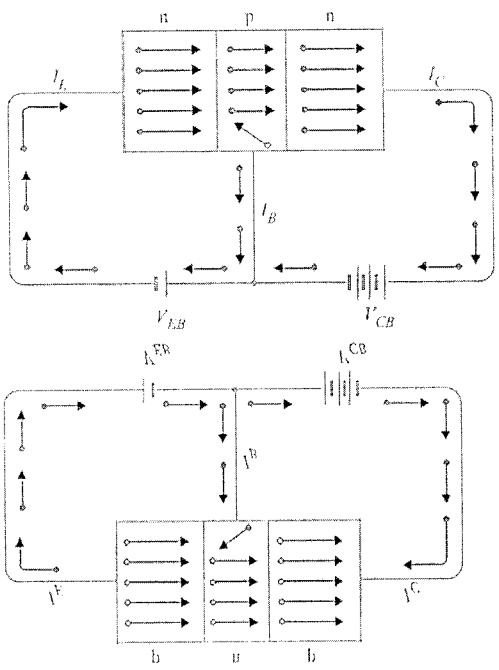
Part A (10Q x 1M = 10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1.	(b) 4 Diodes and Step Down Transformer	1 M	1 min
2.	(c) remove the AC-Ripple Components present in the rectifier output	1 M	1 min
3.	a. $T_2 >> T_1$ hence $T_2 = T$	1 M	1 min
4.	d. with Heavily doped Semiconductor to maintain Constant Voltage Level	1 M	1 min
5.	b. Heavily – Lightly- Moderately Doped	1 M	1 min
6.	b. Emitter-Base Junction is Forward Biased and Collector-Base Junction is Reverse Biased	1 M	1 min
7.	a. $I_E = I_C + I_B$	1 M	1 min

8.	c. $\beta = \frac{\alpha}{1-\alpha}$	1 M	1 min
9.	a. Cut-Off Region :: OFF STATE and Saturation Region :: ON STATE	1 M	1 min
10.	a. $\beta = \frac{IC}{IB}$	1 M	1 min

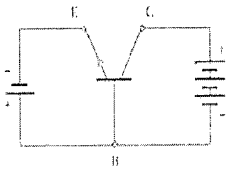
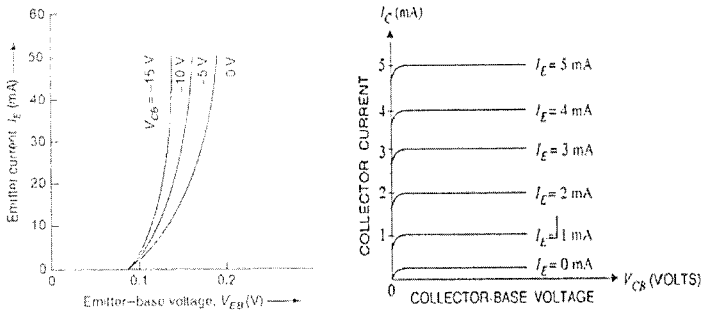
Part B **(2Q x 5M = 10 Marks)**

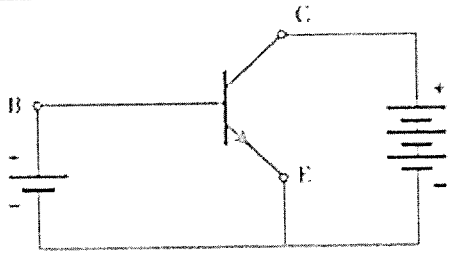
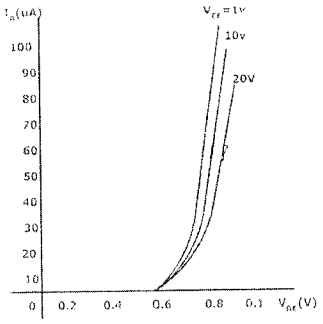
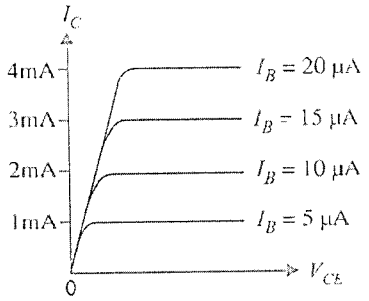
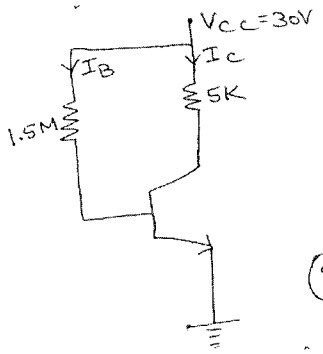
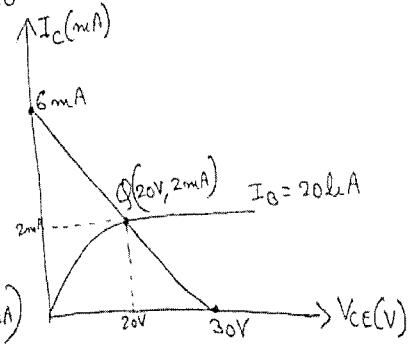
Q No	Solution	Scheme of Marking	Max. Time required for each Question
1.	a) High Electric Field b) ~~Voltage Level constant~~ 10mA c) True d) True e) 0.7V	1 Marks each – 5M	5 Mins
2.	Either PNP/ NPN construction + Terminal Voltage & Currents +explanation 	1+1+2+1= 5 M	10 Mins



Part C

(2Q x 5M = 10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1.	 <u>Characteristics of Common base Connection</u>  Fig. 2.10: i. Input characteristics ii. Output characteristics	2.5M	

	   Fig. 2.13: i Input characteristics ii. Output characteristics	2.5M	15 Mins
2.	 ① Apply KVL in i/p ckt, $I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $= \frac{30V}{1.5M} = 20\mu A$ ② $I_C = \beta I_B = 100 \times 20\mu A$ $= 2mA$ ③ Apply KVL in o/p ckt, $V_{CE} = V_{cc} - I_C R_C = 30 - 2\times5 = 20V$ ④ d.c. loadline points, when $I_C = 0$, $V_{CE} = V_{cc} = 30V$ when $V_{CE} = 0$, $I_C = \frac{V_{cc}}{R_C} = \frac{30}{5K} = 6mA$ Q-point(20V, 2mA)  	2M 3M	15 Mins

Roll No.												

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Semester: Odd Semester: 2019-20 | **Date**: 31 December 2019

Course Code: ECE 101 | **Time**: 01:00PM - 04:00PM

Course Name: Elements of Electronics Engineering | **Max Marks**: 100

Programme & Sem: B.Tech(Chemistry Cycle) & I Semester | **Weightage**: 50%

Instructions:

(i) ***Read Questions carefully and answer accordingly***
(ii) ***Scientific and Non- programmable calculators are permitted***
(iii) ***This question paper contains two pages***

Part A[Memory Recall Questions]

Answer **all** the Questions. **Each** question carries **1** mark.

1. Fill in the blanks with appropriate answers: (15Qx1M=15M)

i. The cut in voltage of Germanium is _____. (C.O.No. 1) [Knowledge]
ii. Efficiency of the full wave rectifier ideally is _____. (C.O.No. 1) [Knowledge]
iii. Rectifier performs conversion of AC to_____. (C.O.No. 2) [Knowledge]
iv. Diode current is large for _____ bias condition. (C.O.No. 1) [Knowledge]
v. In forward bias of pn junction diode, n-type material is connected to _____ terminal of the battery. (C.O.No. 1) [Knowledge]
vi. The current amplification factor in common emitter circuit is _____. (C.O.No. 2) [Knowledge]
vii. The device that transfers a signal from a low resistance to high resistance is called as_____. (C.O.No. 2) [Knowledge]
viii. If the base current is 100μA and the current amplification factor is 100, then the collector current is_____. (C.O.No. 1) [Knowledge]
ix. The 8085 has _____bit data bus. (C.O.No. 4) [Knowledge]
x. The 2's complement of 10101101 is_____. (C.O.No. 3) [Knowledge]
xi. The microprocessor 8085 operates in maximum _____ frequency. (C.O.No. 4) [Knowledge]
xii. The process of changing _____of a carrier Wave in accordance with the intensity of the signal is known as Amplitude modulation. (C.O.No. 4) [Knowledge]
xiii. Microprocessor 8085 can address _____ byte of memory. (C.O.No. 4) [Knowledge]
xiv. De-Morgan's Law is A'+B'=_____. (C.O.No. 3) [Knowledge]

xv. Input Transducer in a communication system converts any form of signal to _____signal. (C.O.No. 4) [Knowledge]

2. Answer the following: **(15Qx1M=15M)**

i. Convert $(105)_{10}$ to binary. (C.O.No. 3) [Knowledge]
ii. Convert $(2FFE)_{16}$ to binary. (C.O.No. 3) [Knowledge]
iii. Find the 10's complement of 012398. (C.O.No. 3) [Knowledge]
iv. Find the 2's complement of 11001101. (C.O.No. 3) [Knowledge]
v. Find the 9's complement of 89894. (C.O.No. 3) [Knowledge]
vi. Add 0101110 & 0101011. (C.O.No. 3) [Knowledge]
vii. For transistor to work as amplifier it is operated in saturation region. State True or False. (C.O.No. 2) [Knowledge]
viii. Use Basic Theorem to write:
A+A'B= (C.O.No. 3) [Knowledge]
ix. State the function of receiver in communication system. (C.O.No. 4) [Knowledge]
x. Give one examples for both input & output transducer. (C.O.No. 4) [Knowledge]
xi. A resistor having value 10KΩ is connected to 50V source. Determine the current in the resistor. (C.O.No. 1) [Knowledge]
xii. The carrier signal in communication has low frequency. State True or False. (C.O.No. 4) [Knowledge]
xiii. If capacitance in filter circuit increases the ripple will increase. State True or False. (C.O.No. 1) [Knowledge]
xiv. Name the only physical connection between a transmiter & receiver. (C.O.No. 4) [Knowledge]
xv. Mention the difference between Static & Dynamic resistance. (C.O.No. 1) [Knowledge]

Part B [Thought Provoking Questions]

Answer **all** the Questions. **Each** question carries **5** marks. **(4Qx5M=20M)**

3. Identify the Transistor Configuration and the regions A, B & C as shown in figure1. Mention the conditions for biasing in each region. (C.O. No. 2) [Comprehension]

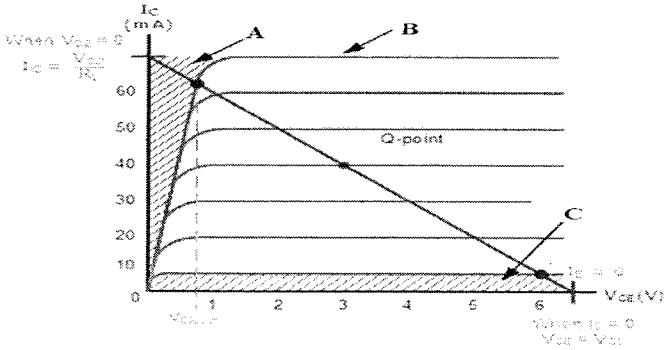


Figure 1

4. Write short notes on 2 diode full-wave rectifier with suitable diagram. Mention its efficiency.
(C.O. No. 1) [Comprehension]

5. State & Prove De-Morgan's theorem with the help of truth table.
(C.O. No. 3) [Comprehension]

6. Derive the following relationships: (i) $\alpha \rightarrow \gamma$ (ii) $\alpha \rightarrow \beta$
(C.O. No. 2) [Comprehension]

Part C [Problem Solving Questions]

Answer all the Questions. Each Question carries 10 marks. (5Qx10M=50M)

7. Write the logic symbol, expression and truth table for the following logic gates

a. NOT b. AND c. OR d. NAND e. NOR f. Ex-OR g. Ex-NOR

(C.O. No. 3) [Comprehension]

8. (a) Form the SOP equation and simplify it for the given function: f(A,B,C) = $\sum$ (7,5,6). Implement the following using AND-OR gates and NAND-NAND gates:
(C.O. No. 3) [Comprehension]

(b) Perform binary subtraction of $(1100110)_2$ and $(110101)_2$ with 2's Complement.

9. Explain with a neat diagram, the block diagram of Communication System.

(b) Define Amplitude modulation (AM) and frequency modulation (FM). Sketch the waveforms of AM & FM. (C.O. No. 4) [Comprehension]

10. State the laws of Boolean algebra (Commutative law, Associative law, Distributive law). Prove each law using truth table method. (C.O. No. 3) [Comprehension]

11. Draw the architecture of 8085 microprocessor and explain the following blocks:

a. ALU b. Stack pointer c. Program counter d. Instruction register

(C.O. No. 4) [Comprehension]

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE REACH GREATER HEIGHTS

Semester: Odd Sem 2019-20

Course Code: ECE 101

Course Name: Elements of Electronics Engineering

Date: 31 December 2019

Time: 3 Hour

Max Marks: 100

Weightage: 50%

Extract of question distribution [outcome wise & level wise]

Q.NO	C.O.NO (%age of CO)	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	A	
Q 1.	CO1,CO 2	Module 1,2,3,4	15			15
Q 2.	CO1,CO 2	Module 1,2,3,4	15			15
Q 3.	CO 2	Module 2		5		5
Q 4.	CO 2	Module 2		5		5
Q 5.	CO 2	Module 3		5		5
Q 6.	CO 2	Module 2		5		5
Q 7.	CO 2	Module 3			10	10
Q 8.	CO 2	Module 3			10	10
Q 9.	CO 2	Module 4			10	10
Q 10.	CO 2	Module 3			10	10
Q 11.	CO 2	Module 4			10	10
	Total Marks		30	20	50	100

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

I hereby certify that all the questions are set as per the above guidelines. [Maitraiyee Konar]

Reviewer's Comments:

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SCHOOL OF ENGINEERING

SOLUTION

Semester: Odd Sem 2019-20

Course Code: ECE 101

Course Name: Elements of Electronics Engineering

Date: 31 December 2019

Time: 3 Hour

Max Marks: 100

Weightage: 50%

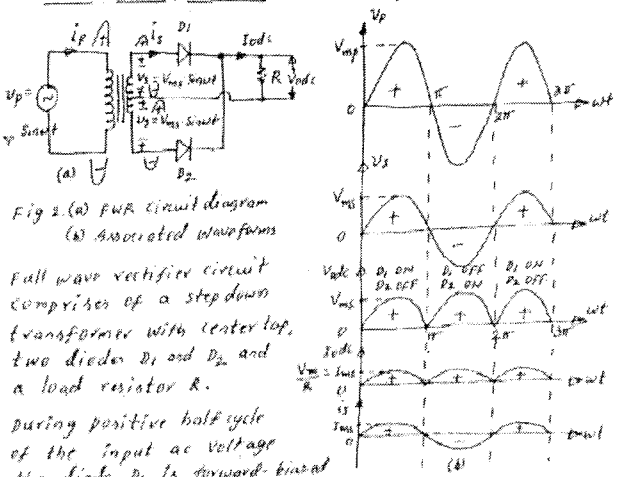
Part A (30Q x 1M = 30Marks)

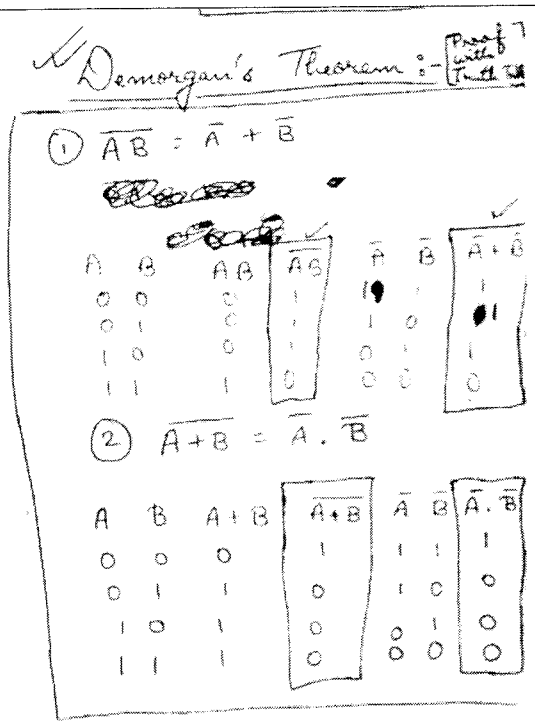
Q No	Solution	Scheme of Marking	Max. Time required for each Question
Q 1)	(i) 0.3V (ii) 81.2% (iii) Pulsating DC (iv) Forward (v) Negative (vi) β (vii)Transistor (viii) 10mA (ix) 8 bit (x) 01010011 (xi) 3MHz (xii)Amplitude (xiii) 64K (xiv) (AB)' (xv) Electrical	1M each	17min

Q 2.	(i) 1101001 (ii) 0010111111111110 (iii) 987602 (iv) 00110011 (v) 10105 (vi) 1011001 (vii)False (viii) A+B (ix) Extract message signal from modulated signal. (x) Microphone, Loudspeaker (xi) 5mA (xii)False (xiii) False (xiv) Channel (xv) Static- V/I Dynamic- ΔV/ΔI	1M each	18min

Part B (4Q x 5M = 20Marks)

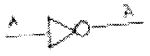
Q No	Solution	Scheme of Marking	Max. Time required for each Question
Q 3)	CE configuration A- Saturation B- Active C- Cut-off Saturation Region: Both the junctions are in forward bias condition. Active Region: Input junction is forward bias while output junction is reverse bias Cut- off Region: Both the junctions are in reverse bias condition.	0.5M 0.5M +0.5M+0.5M 1M+1M+1M	15min

Q 4)	1. Full wave Rectifier (Two Diodes) : (12)  Fig 2 (a) FWR circuit diagram (b) Associated waveforms Full wave rectifier circuit comprises of a step down transformer with center tap, two diodes D_1 and D_2 and a load resistor R. During positive half cycle of the input ac voltage the diode D_1 is forward-biased and conducts, where as diode D_2 is reverse-biased and do not conducts the current flows along a path $V_s - D_1 - R - V_s$. As a result positive half cycle is dropped across load resistor R. During negative half cycle of the input ac voltage the	1M+1M+2M+1M	15min
Q 5)	Prove De-Morgans Theorem with truth table	2.5M+2.5M	15min

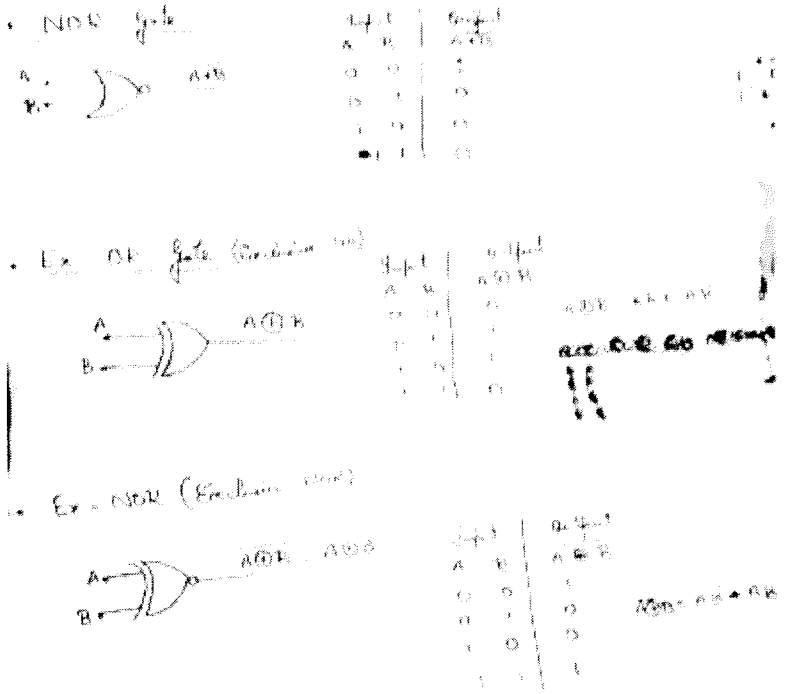
Q 6)	 Derive the relations: $\alpha \rightarrow \gamma$ (ii) $\alpha \rightarrow \beta$ **Relation between γ and α** $\gamma = \frac{\Delta I_E}{\Delta I_B}$ ---------- (i) $\alpha = \frac{\Delta I_C}{\Delta I_E}$ ---------(ii) Now $I_E = I_B + I_C$ or $\Delta I_E = \Delta I_B + \Delta I_C$ or $\Delta I_B = \Delta I_E - \Delta I_C$ Substituting the value of ΔI_B in exp. (i) we get, $\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$ Dividing the numerator and denominator of R.H.S. by ΔI_E we get, $\gamma = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha}$ $\left(\because \alpha = \frac{\Delta I_C}{\Delta I_E}\right)$ $\therefore \gamma = \frac{1}{1-\alpha}$ Relation between β and α. A simple relation exists between β and α. This can be derived as follows : $\beta = \frac{\Delta I_C}{\Delta I_B}$ (i) or $\beta = \frac{\Delta I_C}{\Delta I_E}$ (ii) Now $I_E = I_B + I_C$ or $\Delta I_E = \Delta I_B + \Delta I_C$ or $\Delta I_B = \Delta I_E - \Delta I_C$ Substituting the value of ΔI_B in exp. (i) we get,	2.5M+2.5M	15min

	 $\beta = \frac{I_c}{I_E - I_c}$ ... (iii) Dividing the numerator and denominator of R.H.S. of eqn (iii) by I_E, we get $\beta = \frac{\frac{I_c}{I_E}}{\frac{I_E}{I_E} - \frac{I_c}{I_E}} = \frac{\alpha}{1-\alpha}$ $\left[\because \alpha = \frac{I_c}{I_E}\right]$ $\beta = \frac{\alpha}{1-\alpha}$		

Part C (5Q x10M = 50Marks)

Q No	Solution	Scheme of Marking	Ma Time required for each Question
Q 7)	Digital logic Gates → There are 3 basic logical operators NOT, AND, OR • NOT / Inverter Gate  Input: (Low) 0, (High) 1 | Output: 1 (High), 0 (Low) • AND gate  Input: A, B: 0 0 / 0 1 / 1 0 / 1 1 | output A.B: 0 0 0 1 • OR gate  Input: A, B: 0 0 / 0 1 / 1 0 / 1 1 | output A+B: 0 1 1 1	1M+(1.5Mx6)	15min

Q 8)
(a)



1M+2M

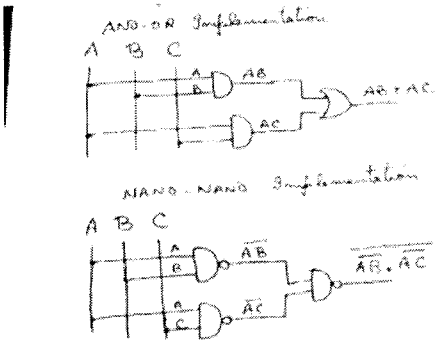
$f(A,B,C) = \sum m(2,5,6)$

$A\bar{B}C + AB\bar{C} + A\bar{B}\bar{C}$

$AC(\bar{B}+B) + A\bar{B}\bar{C}$

$AC + A\bar{B}\bar{C} = A(C + \bar{C}\bar{B}) = A(\bar{B}+C) = AB + AC$

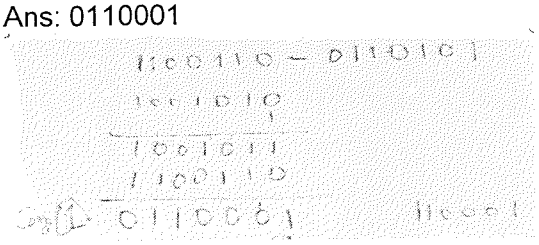
15min



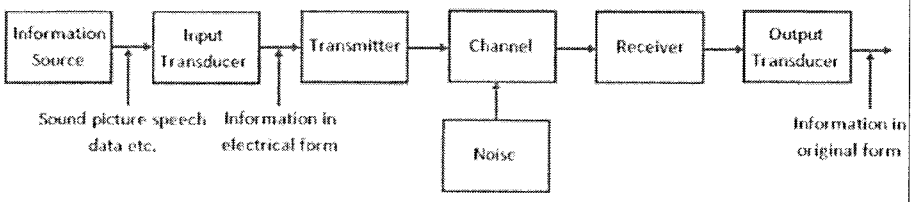
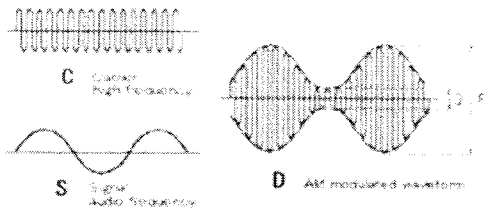
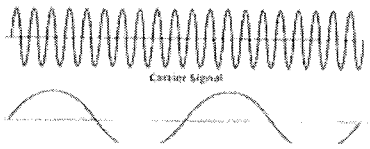
2M+2M

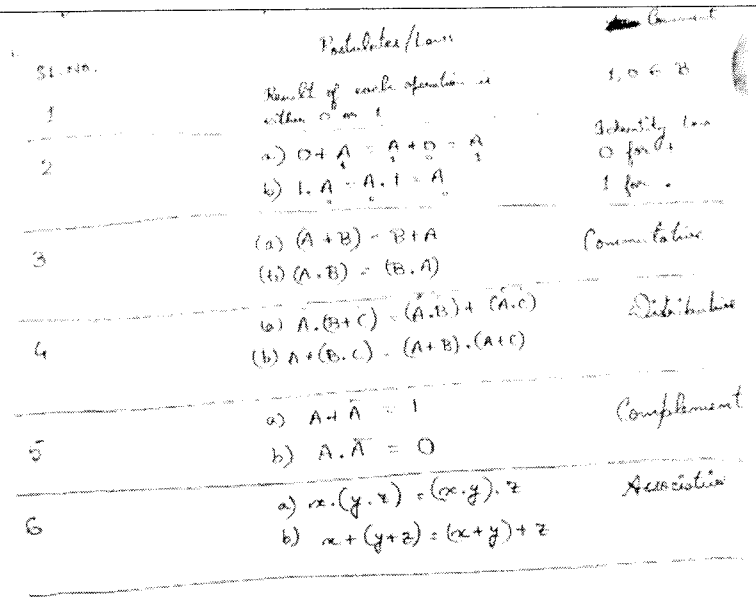
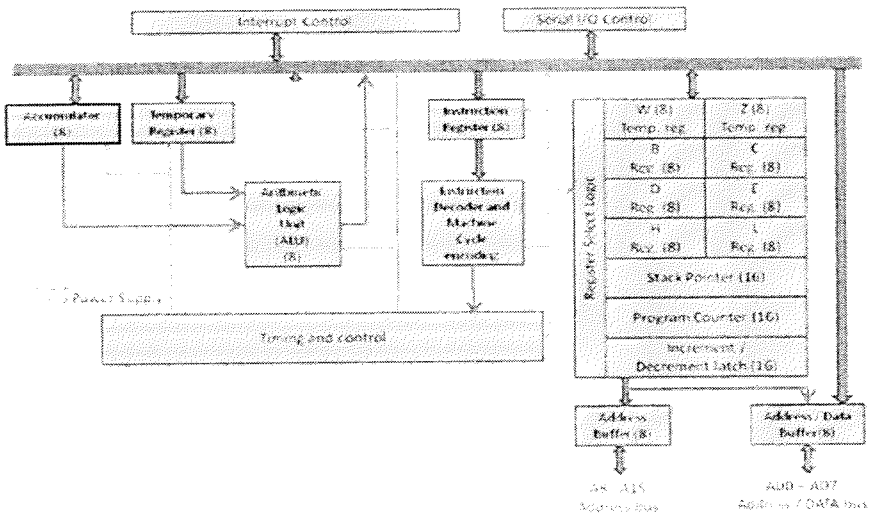
(b)

Ans: 0110001



3M

Q 9) (a)	 Fig 1 communication system block diagram Explain each block	2M+4M	15min
(b)	**(i)Amplitude Modulation** When the amplitude of high frequency carrier wave is changed in accordance with the intensity of the signal, it is called amplitude modulation.  22 Elements of Electronics Engineering 2017 In amplitude modulation, only the amplitude of the carrier wave is changed in accordance with the intensity of the signal and the frequency of the modulated wave remains the same i.e. carrier frequency. **Frequency Modulation (FM)** When the frequency of carrier wave is changed in accordance with the intensity of the signal, it is called frequency modulation (FM). In frequency modulation, only the frequency of the carrier wave is changed in accordance with the signal and the amplitude of the modulated wave remains the same i.e. carrier wave amplitude.  	4M	
Q 10)	Prove Laws of Boolean Algebra	5M+2.5M+2.5M	15min

Q 11)	  ALU- Performs Arithmetic & Logic Operations Stack Pointer- 16-bit register used as a memory pointer. Program counter- Deals with sequencing the instructions of program. Instruction Register-Temporary store current instruction of a program	6M+4M	15min