Roll No.													

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST 1

Sem & AY: Odd Sem. 2019-20
Course Code: CSE 202
Course Name: DIGITAL DESIGN
Program & Sem: B.Tech & III

Date: 30.09.2019
Time: 11:00AM to 12:00PM
Max Marks: 40
Weightage: 20%

Instructions:
i. Write the Questions legibly
ii. All Questions are compulsory.

Part A [Memory Recall Questions]

Answer all the Questions. Each Question carries five Marks. (2Qx5M=10M)

1. State and Prove De-Morgan's theorem (C.O.NO.1) [Knowledge]

2. Write HDL Code for the following Circuit shown in Fig. 01 (C.O.NO.1) [Application]

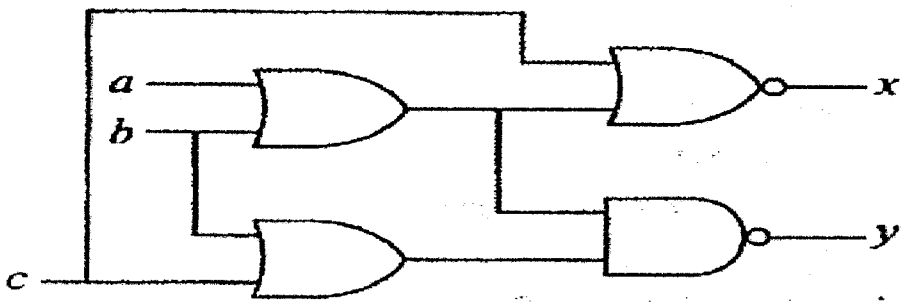

Fig. 01

Part B [Thought Provoking Questions]

Answer all the Questions. Each Question carries ten marks. (2Qx10M=20M)

3. By applying Boolean Algebra Theorems and Postulates. Minimize the following Boolean Expressions to a minimum number of Literals.

(C.O.NO.1) [Comprehension]

a. x+x'y b. x(x'+y) c. (x+y)(x'+z)(y+z)
d. (x+y)(x+y') e. xy+x'z+yz

4. For the following Boolean Function, obtain the simplified expression using K-MAP method. Also draw the logic diagram for the obtained Simplified expression.

$F(a,b,c,d) = \sum(0,1,5,7,8,10,14,15)$ (C.O.NO.2) [Application]

Part C [Problem Solving Questions]

Answer the Question. The Question carries ten marks. **(1Qx10M=10M)**

5. Consider the following Boolean expression. (C.O.NO.2) [Application]

$F(w,x,y,z) = \sum m(1,3,7,11,15) + d(0,2,5)$

Using K-Map method, obtain the simplified expression

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

Semester: 3rd
Course Code: CSE 202
Course Name: Digital design

Date: 30/09/2019
Time: 11:30 am to 12:30 pm
Max Marks: 40 Marks
Weightage: 20%

Extract of question distribution [outcome wise & level wise]

Q.NO.	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	A	
1	1	Module-1	5			5
2	1	Module-1			5	5
3	1	Module-1	10			10
4	2	Module-2			10	10
5	2	Module-2			10	10
	Total Marks		15		25	40

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

[I hereby certify that All the questions are set as per the above guide lines. Mr. K Ramakrishna]

Reviewers' Comments

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

SOLUTION

Semester: 3rd sem
Course Code: CSE 202
Course Name: Digital design

Date: 30/09/2019
Time: 11:30 am to 12:30 pm
Max Marks: 40 Marks
Weightage: 20%

Part A (2Q x5 M =10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	**De Morgan's Theorem – There are two "de Morgan's" rules or theorems,** **(1) Two separate terms NOR'ed together is the same as the two terms inverted (Complement) and AND'ed for example:** $("A + B")^{-} = "A"^{-} . "B"^{-}$ **(2) Two separate terms NAND'ed together is the same as the two terms inverted (Complement) and OR'ed for example:** $("A . B")^{-} = "A"^{-} + "B"^{-}$	**Complete proof 5M**	**5 Mins**

A	B	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A} + \overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

2	**module eg2(a,b,c,x,y);** **input a,b,c;** **output x,y;** **wire or_op1, or_op2;** **or g1(or_op1,a,b);** **or g2(or_op2,b,c);** **nor g13(x,c,or_op1);** **nand g4(y,or_op1,or_op2);** **endmodule**	**Full Code 5M**	**5 Mins**

Part B (2Q x10 M =20 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
3	Simplify the following Boolean functions to a minimum number of literals. 1. $x(x' + y) = xx' + xy = 0 + xy = xy$. 2. $x + x'y = (x + x')(x + y) = 1(x + y) = x + y$. 3. $(x + y)(x + y') = x + xy + xy' + yy' = x(1 + y + y') = x$. 4. $xy + x'z + yz = xy + x'z + z(x + x')$ $= xy + x'z + xyz + x'yz$ $= xy(1 + z) + x'z(1 + y)$ $= xy + x'z$. 5. $(x + y)(x' + z)(y + z) = (x + y)(x' + z)$, by duality from function 4.	2M for each correct answer	10 Mins
4	F(a,b,c,d) = ∑(0,1,5,7,8,10,14,15) Simplified expression: **b'c'd' + a'c'd + bcd + acd'**	K-map – 2M Grouping – 2M	15 Mins

		Simplified expression – 4M Correct logic diagram – 2M	

Part C (1Q x10 M =10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
5	F(w,x,y,z) = ∑m(1,3,7,11,15) + d(0,2,5) Ans: **yz + w'x' OR yz + w'z**	K-map – 2M Grouping – 3M Simplified expression – 5M	15 Mins

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BENGALURU

SCHOOL OF ENGINEERING

TEST – 2

Sem & AY: Odd Sem 2019-20
Course Code: CSE 202
Course Name: DIGITAL DESIGN
Program & Sem: B.Tech (CSE/CCE/ISE/IST) & III

Date: 18.11.2019
Time: 11.00 AM to 12.00 PM
Max Marks: 40
Weightage: 20%

Instructions:

i. *Write the Questions legibly.*
ii. *All Questions are compulsory.*

Part A [Memory Recall Questions]

Answer all the Questions. Each sub Question carries one mark. (10Qx1M=10M)

1. Fill in the blanks:
   a) If A, B and C are the inputs of a full adder then the sum is given by _____ (C.O.NO.2)[Knowledge]

   b) In a multiplexer, the selection of a particular input line is controlled by _____ (C.O.NO.2)[Knowledge]
   c) In 1-to-4 multiplexer, C1 and C2 are select lines and if C1 = 1 & C2 = 1, then the output will be _____ (C.O.NO.2)[Knowledge]
   d) _____ technique will be used to convert a higher configuration MUX to a lower one (C.O.NO.2)[Knowledge]
   e) ___ , ____ and _____ number of AND, OR and XoR gates respectively, are required for the configuration of a FULL-ADDER (C.O.NO.2)[Knowledge]
   f) In octal to binary encoder, _____ number of outputs will be generated (C.O.NO.2)[Knowledge]
   g) _____ gate can be used as a Basic comparator (C.O.NO.2)[Knowledge]
   h) For binary number 1010, _____ is the equivalent gray code (C.O.NO.2)[Knowledge]
   i) In QM method, _____ are examined to get _____ for a particular expression that avoids any type of duplication (C.O.NO.2)[Knowledge]
   j) _____ combinational circuit is also known as "Data Distributor" (C.O.NO.2)[Knowledge]

Part B [Thought Provoking Questions]

Answer both the Questions. Each Question carries eight marks. (2Qx8M=16M)

2. Explain the working of 8:1 MUX. Construct 8:1 MUX using only 2:1 Mux.

(C.O.NO.2)[Comprehension]

3. Design a combinational circuit to convert the given 4-bit BCD code to Excess-3 code. Write the Truth Table, Boolean expressions and Logic diagram for the same.

(C.O.NO.2)[Comprehension]

Part C [Problem Solving Questions]

Answer the Question. The Question carry fourteen marks. (1Qx14M=14M)

4. List the steps involved in determining prime implicants in Quine McClusky Method.

Using Quine McClusky Method, obtain the simplified expression for the following Boolean function: (C.O.NO.2)[Application]

$$Y = F(A, B, C) = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + \overline{A}BC + A\overline{B}C$$

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

Semester: III
Course Code: CSE 202
Course Name: Digital design

Date: 18/11/2019
Time: 1 Hour
Max Marks: 40 Marks
Weightage: 20%

Extract of question distribution [outcome wise & level wise]

Q.NO	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	A	
1	CO 2	Module-2	10			10
2	CO 2	Module-2		8		8
3	CO 2	Module-2		8		8
4	CO 2	Module-2			14	14
	Total Marks		10	16	14	40

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

SCHOOL OF ENGINEERING

SOLUTION

Date: 18/11/2019

Time: 1 Hour

Max Marks: 40 Marks

Weightage: 20%

Semester: III

Course Code: CSE 202

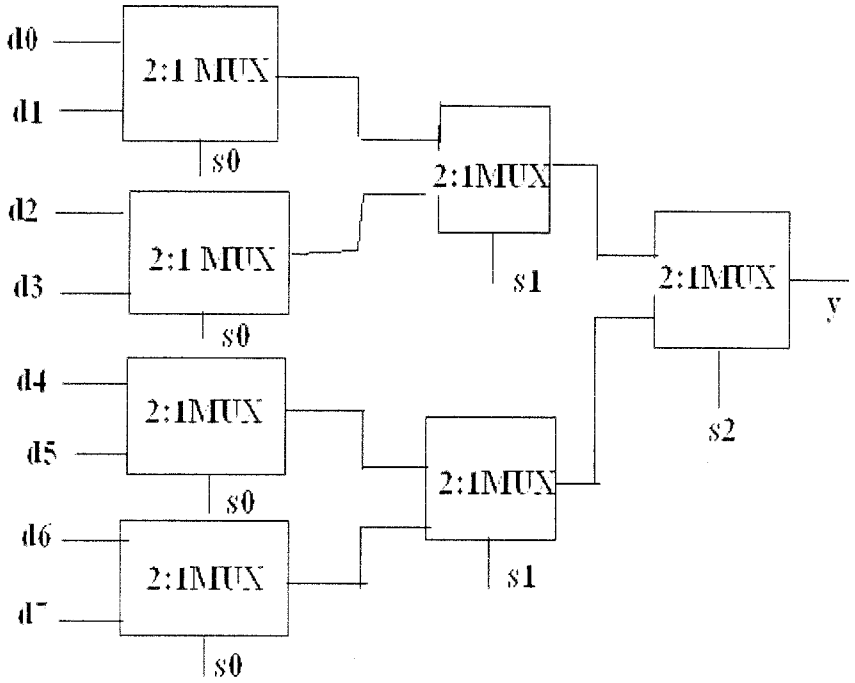
Course Name: Digital design

Part A (10 Q x1 M =10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	A) A XOR B XOR C B) SELECT LINES C) Y3 (4^{th} input line) D) MEV E) 2,1,2 F) 3 G) XOR H) 1111 I) PRIME IMPLICANT, ESSENTIAL PRIME IMPLICANT J) DEMUX	Each correct answer carries 1M	10 Mins

Part B

(2Q x8 M =16 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
2	Explanation of 8:1 MUX using block diagram. Construct 8:1 MUX using 2:1 MUX only 	Explanation with block diagram 3M 16:1 using 4:1 MUX 5M	15 Mins
3	Design a combinational circuit to convert the given 4-bit BCD code to Excess-3 code. Write the Truth Table, Boolean expressions and Logic diagram for the same. Input BCD / Output Excess-3 Code A B C D | w x y z 0 0 0 0 | 0 0 1 1 0 0 0 1 | 0 1 0 0 0 0 1 0 | 0 1 0 1 0 0 1 1 | 0 1 1 0 0 1 0 0 | 0 1 1 1 0 1 0 1 | 1 0 0 0 0 1 1 0 | 1 0 0 1 0 1 1 1 | 1 0 1 0 1 0 0 0 | 1 0 1 1 1 0 0 1 | 1 1 0 0	Boolean expressions: 4M Truth Table 4M	15 Mins

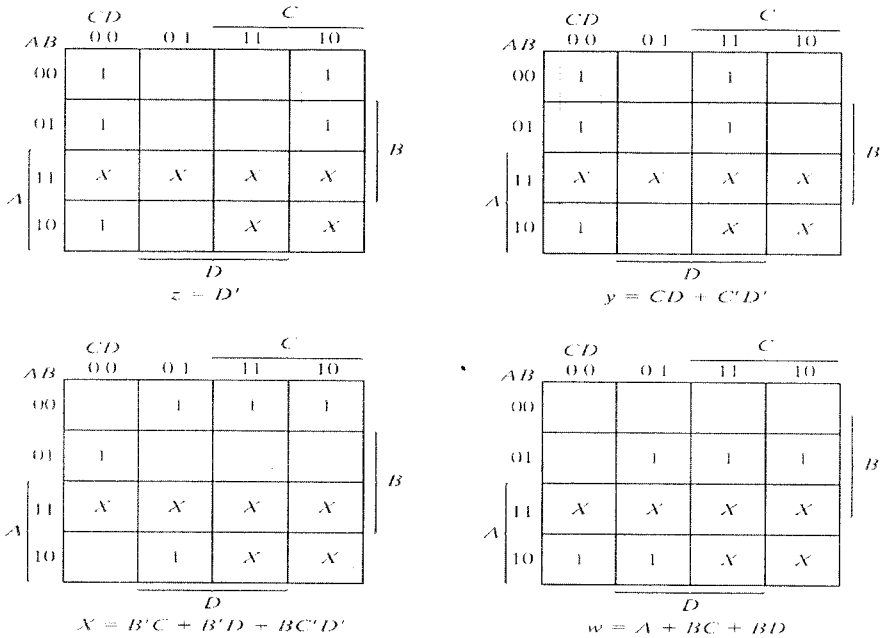
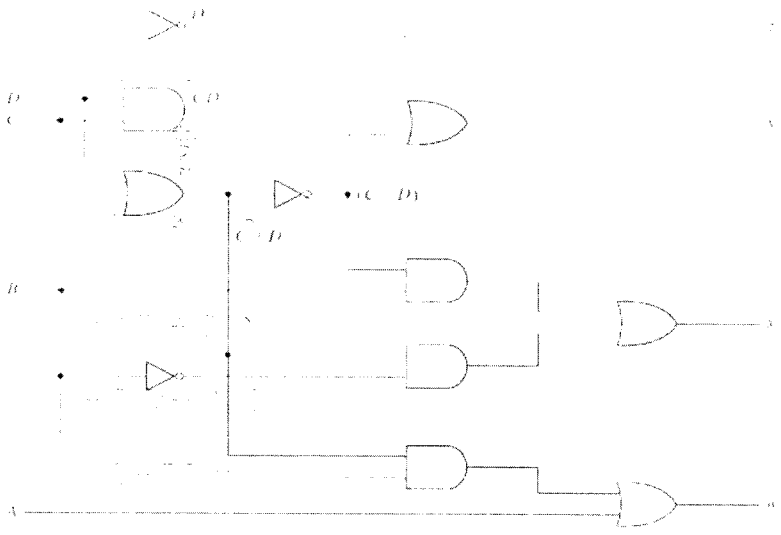


Fig. 4-3 Maps for BCD to Excess-3 Code Converter

$z = D'$; $y = CD + C'D' = CD + (C + D)'$

$x = B'C + B'D + BC'D' = B'(C + D) + B(C + D)'$

$w = A + BC + BD = A + B(C + D)$



Part C (1Q x14 M =14 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
4	Steps involved Determination of Prime Implicants • In Stage 1 of the process, to find out all the terms that gives output 1 from truth table and put them in different groups depending on how many 1s input variable combinations *(ABCD)* have. • For example, first group has no 1 in input combination, second group has only one 1, third two 1 s, fourth three 1s and fifth four 1s. • In Stage 2, we first try to combine first and second group of Stage I, on a member to member basis. • The rule is to see if only one binary digit is differing between two members and we mark that position by '–'. This means corresponding variable is not required to represent those members. • Thus (0) of first group combines with (1) of second group to form (0,1) in Stage 2 and can be represented by *A'B'C'* (0 0 0 –). • Proceed in the same manner to find rest of the combinations in successive groups of Stage 1 and table them as in figure. • Note that, we need not look beyond successive groups to find such combinations as groups that are not adjacent, differ by more than one binary digit. Also note that each combination of Stage 2 can be represented by three literals. • All the members of particular stage, which finds itself in at least one combination of next stage are tick (√) marked. This is followed for Stage 1 terms as well as terms of other stages.	Steps Involved: 5M PI Table 4M EPI Table 3M Correct simplified expression 2M	15 Mins

$Y = F(A, B, C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C$

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Stage 1			Stage 2	
ABC			ABC	
000	(0)	√	00–	(0, 1)
001	(1)	√	0–1	(1, 3)
			–01	(1, 5)
011	(3)	√		
101	(5)	√		

Prime implicants only from stage 2
They are:
00–($A'B'$), 0–1 ($A'C$) and –01 ($B'C$)

	0	1	3	5
$A'B'$	√	√		
$A'C$		√	√	
$B'C$		√		√

All are essential
$Y = A'B' + A'C + B'C$

Roll No												

GAIN MORE KNOWLEDGE
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PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Semester: Odd Sem: 2019 - 20
Course Code: CSE 202
Course Name: DIGITAL DESIGN
Program & Sem: B.Tech, (CSE/IST/ISE/CCE) & III

Date: 24 December 2019
Time: 1:00 PM to 4:00 PM
Max Marks: 80
Weightage: 40%

Instructions:
(i) Read the all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.

Part A [Memory Recall Questions]

Answer all the Questions. Each Question carries 1 mark. (15Qx1M=15M)

1. (i). How many variables will be eliminated by an octet in a 4 variable K Map? (C.O.No.1) [Knowledge]

(ii). A single variable within a term which may or may not be complemented is known as --- (C.O.No.1) [Knowledge]

(iii). 'n' variables can be combined to form ---------- number of minterms. (C.O.No.1) [Knowledge]

(iv). Sum-of-minterms form of F(A,B,C) = AB' + B'C is ---------- (C.O.No.1) [Knowledge]

(v). ---------- is used to increase the effective size of K MAP by writing output in terms of input. (C.O.No.1) [Knowledge]

(vi). How many half adder(s) and OR gate(s) are required to implement a full adder? (C.O.No.2) [Knowledge]

(vii). Octal-to-Binary conversion is an application of ---------- circuit. (C.O.No.2) [Knowledge]

(viii). Excess-3 code for the BCD '1001' is ----------. (C.O.No.2) [Knowledge]

(ix). A 16 ×1 Multiplexer can be constructed with two ---------- and one ---------- multiplexers (C.O.No.2) [Knowledge]

(x). Decoder with enable input can function as a --------- (C.O.No.2) [Knowledge]

(xi). A connection from the output of one gate to the input of a second gate whose output forms part of the input to the first gate is called ---------- (C.O.No.3) [Knowledge]

(xii). Latches are built from --------- and flip flops are built from --------(C.O.No.3) [Knowledge]

(xiii). Which flip flop descriptor is used for the design of sequential circuits? (C.O.No.3) [Knowledge]

(xiv). How many unique data patterns are generated by a 4-bit Johnson counter? (C.O.No.3) [Knowledge]

(xv). What is the characteristic equation of T flip flop? (C.O.No.3) [Knowledge]

Part B [Thought Provoking Questions]

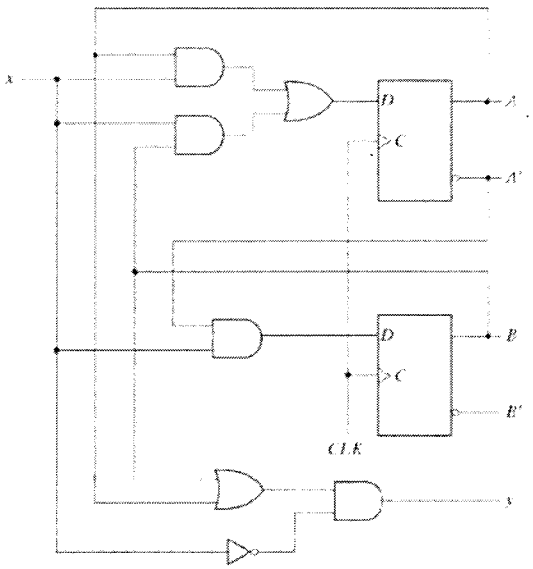
Answer all the Questions. Each Question carries 11 marks. (3Qx11M=33M)

2. Implement the given Boolean function with 4 ×1 multiplexer and external gates.

   $F(A,B,C,D) = \sum m\ (3, 5, 6, 13, 14, 15)$ (C.O.No.2) [Application]

3. Give the simplest logic circuit for following logic equation after the simplification using K Map. *d* represents don't-care condition.
   $F(A,B,C,D) = \sum m(4, 5, 7, 8, 10, 13) + d(0, 1, 2, 9, 12)$ (C.O.No.2) [Comprehension]

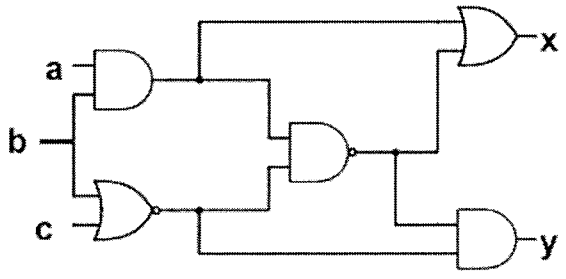
4. Analyze the given circuit and obtain the state transition diagram. (C.O.No.3) [Comprehension]



Part C [Problem Solving Questions]

Answer both the Questions. Each Question carries 16 marks. (2Qx16M=32M)

5. Write a Verilog code for the given circuit. Also simplify the expression for outputs using Boolean algebra. (C.O.No.1) [Comprehension]



6. List the steps for designing synchronous sequential circuits. Design a 3-bit synchronous binary down counter using T flip flop. (C.O.No.3) [Application]

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Extract of question distribution [outcome wise & level wise]

Q.NO.	C.O.NO (% age of CO)	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	A	
1	1,2,3	1,2,3	15	-	-	15
2	2	2	-	-	11	11
3	2	2	-	11	-	11
4	3	3	-	11	-	11
5	1	1	-	16	-	16
6	3	3	-	-	16	16
	Total Marks		15	38	27	80

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

I hereby certify that all the questions are set as per the above guidelines.

Faculty Signature: SHIMIL SHIJO

Reviewer Commend:

Format of Answer Scheme

SCHOOL OF ENGINEERING

SOLUTION

Semester: Odd Sem. 2019-20
Course Code: CSE 202
Course Name: DIGITAL DESIGN
Program & Sem: B.TECH, III CSE/IST/ISE/CCE

Date: 24.12.2019
Time: 3 HRS
Max Marks: 80
Weightage: 40%

Part A

(15Q x 1M = 15Marks)

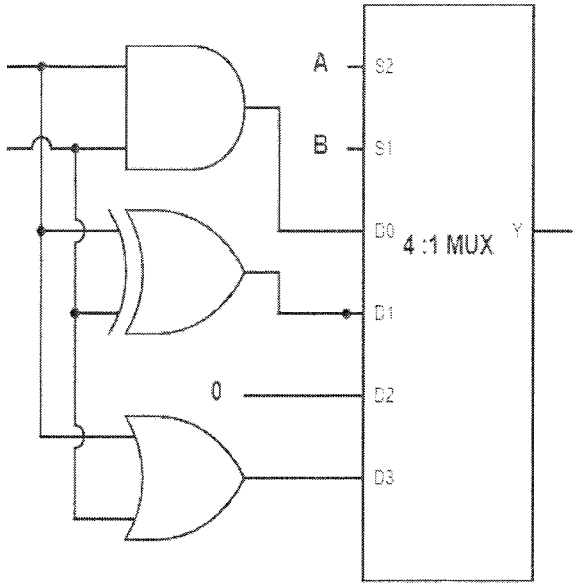
Q No	Solution	Scheme of Marking	Max. Time required for each Questio
1	i. 3 ii. Literal iii. 2^n iv. AB'C + AB'C' + A'B'C v. MEV Technique vi. 2, 1 vii. Encoder viii. 1100 ix. 8 × 1, 2×1 x. Demultiplexer xi. Feedback path xii. Logic gates, Latches xiii. Excitation table xiv. 8 xv. $Q_{n+1} = Q_nT' + Q_n'T$	15Q × 1M = 15 Marks	**20 mins**

Part B

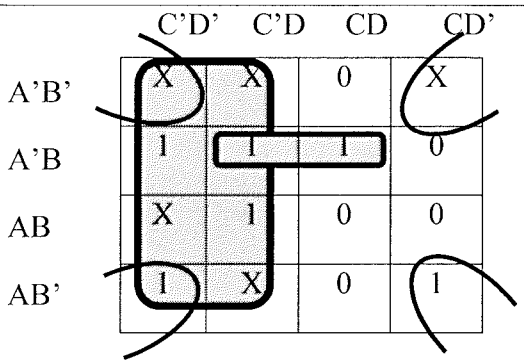
(3Q x 11M = 33 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
2	A B C D F MAP ENTRY 0 0 0 0 0 D_0 0 0 0 1 0 F = CD 0 0 1 0 0 0 0 1 1 1 0 1 0 0 0 D_1 0 1 0 1 1 F = C ⊕ D 0 1 1 0 1 0 1 1 1 0	TRUTH TABLE -2M GROUPING – 2M MAP ENTRY EXPRESSION = 4M LOGIC DIAGRAM - 3M	30 mins

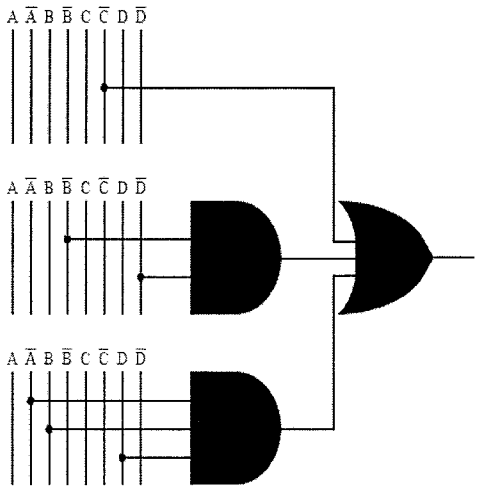
									(2+2 + 4 + 3 = 11 MARKS)	
	1	0	0	0	0	D_2 F = 0				
	1	0	0	1	0					
	1	0	1	0	0					
	1	0	1	1	0					
	1	1	0	0	0	D_3 F= C + D				
	1	1	0	1	1					
	1	1	1	0	1					
	1	1	1	1	1					

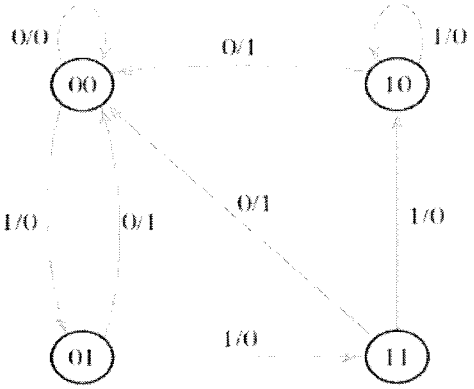


3.									2 Marks – K Map 3 Marks – Grouping (Rolling and overlapping groups) 3 Marks – Expression 3 Marks - Circuit (2+3+3+3= 11 Marks)	30 mins



F = C' + B'D'+ A'BD

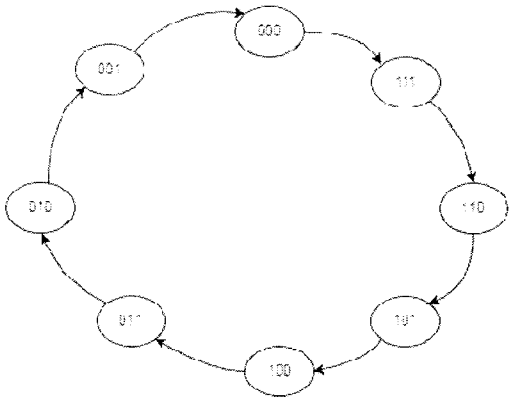


4.	$A(t+1) = D_A = Ax + Bx$ $B(t+1) = D_B = A'x$ $y = (A' + B)\,x'$ **Present State** (A B) / **Input** (x) / **Next State** (A B) / **Output** (y) 0 0 0 → 0 0 0 0 0 1 → 0 1 0 0 1 0 → 0 0 1 0 1 1 → 1 1 0 1 0 0 → 0 0 1 1 0 1 → 1 0 0 1 1 0 → 0 0 1 1 1 1 → 1 0 0 	Boolean Expression - 3M State Table - 4M State Diagram - 4M (3 + 4 + 4 = 11M)	30 mins

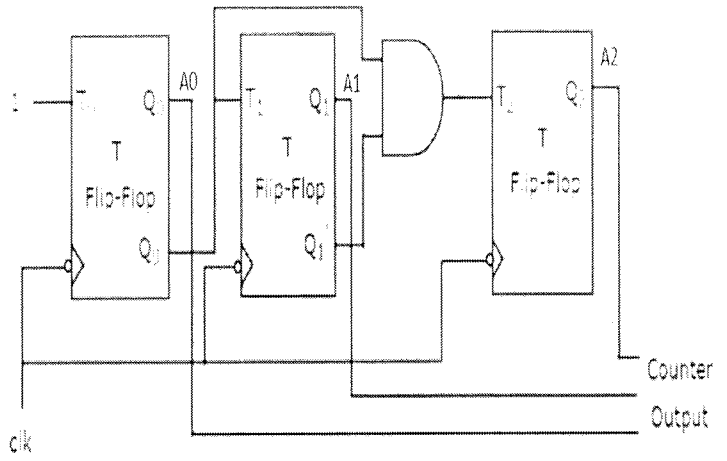
Part C (2Q x 16M = 32Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question

5.	**Verilog Code**
	module ckt(a,b,c,x,y);
	input a.b.c;
	output x,y;
	wire g1_out,g2_out,g3_out;
	and g1(g1_out,a,b);
	nor g2(g2_out,b,c);
	nand g3(g3_out,g1_out,g2_out);
	or g4(x,g1_out,g3_out);
	and g5(y,g2_out,g3_out);
	endmodule
		Verilog Code – 6M
		
		Expression for x -5M
		
		Expression for y -5M
		
		(6 + 5 + 5 = 16 Marks)
			35 mins

	x = (a.b) + ((a.b) . (b + c)')' = (a.b) + (a.b)' + (b+c) = 1 + (b+c) = 1 y = ((a.b) . (b + c)')'. (b+c)' = ((a.b)' + (b+c)). (b+c)' = (a.b)'.(b+c)' = (a' + b') (b'.c') = a'b'c' + b'c' = (a' + 1) b'c' = b'c'		
6.	**Design Procedure** 1. From the word description and specifications of the desired operation, derive a state diagram for the circuit. 2. Reduce the number of states if necessary. 3. Assign binary values to the states. 4. Obtain the binary-coded state table. 5. Choose the type of flip-flops to be used. 6. Derive the simplified flip-flop input equations and output equations. 7. Draw the logic diagram.  T2 = A'$_1$A'$_0$, T1 = A$_0$' , T0 = 1	Design Procedure – 5M State Diagram – 2M State Table – 3M K Map & Expression - 3M Logic Diagram – 3M (5 +2 + 3 + 3 + 3 = 16M)	35 mins

PS			NS			INPUTS		
A2	A1	A0	A2	A1	A0	T2	T1	T0
1	1	1	1	1	0	0	0	1
1	1	0	1	0	1	0	1	1
1	0	1	1	0	0	0	0	1
1	0	0	0	1	1	1	1	1
0	1	1	0	1	0	0	0	1
0	1	0	0	0	1	0	1	1
0	0	1	0	0	0	0	0	1
0	0	0	1	1	1	1	1	1


1
T
Flip-Flop
A0
T
Flip-Flop
A1
T
Flip-Flop
A2
Counter
Output
clk