Roll No.													

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST 1

Sem AY: Odd Sem 2019-20
Course Code: CSE 223
Course Name: COMPUTER ORGANIZATION
Program & Sem: B .Tech (CSE) & III

Date: 01.10.2019
Time: 11.00AM to12.00PM
Max Marks: 40
Weightage: 20%

Instructions:

(i) All the questions are mandatory
(ii) Only Scientific Calculators are allowed

Part A [Memory Recall Questions]

Answer the Question. The Question carries six marks. (1Qx6M=6M)

1 Describe each parameter of the Basic Performance Equation. (C.O.NO.1)[Knowledge]

Part B [Thought Provoking Questions]

Answer both the Questions. Each Question carries ten marks. (2Qx10M=20M)

2. Explain basic instruction types with an example. (C.O.NO.1)[Knowledge]

3. With a neat diagram describe the connections between processor and memory

(C.O.NO.1)[Comprehension]

Part C [Problem Solving Questions]

Answer the Question. The Question carries fourteen marks. **(1Qx14M=14M)**

4 .Represent the following pairs of signed decimal numbers in 4 bit 2's complement numbers and add them. State whether overflow occurs or not.

a) +2 and +3

b) -1 and -3

c) +5 and +6

d) -4 and -7

e) +1 and +4

f) -3 and +7

g) +4 and +3 (C.O.NO.1)[Application]

SCHOOL OF ENGINEERING

Semester: 3

Course Code: CSE223

Course Name Computer Organization

Date: 1st Oct 2019

Time: 1 Hour

Max Marks: 40

Weightage: 20%

Extract of question distribution [outcome wise & level wise]

Q.NO	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [20] Knowledge and Comprehension			Thought provoking type [10] Comprehension			Problem Solving type [10] Knowledge			Total Marks
			K			C			A			
1	1	1	10									10
2	2	2	10									10
3	2	2				10						10
4	1	1							10			10
	Total Marks		20			10			10			40

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

[I hereby certify that All the questions are set as per the above guide lines.

Mr. Shashidhar V]

Reviewers' Comments

SCHOOL OF ENGINEERING

SOLUTION

Semester: 3

Course Code: CSE 223

Course Name :Computer Organization

Date: 1/10/19

Time: 1 Hr

Max Marks: 40

Weightage: 20

Part A (2Q x10 M =20 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	To perform a given task, an appropriate program consisting of a list of instructions is stored in the memory. Figure shows how the memory and the processor can be connected.	Diagram 4 marks 6 Registers 1 mark each .	15 Minutes

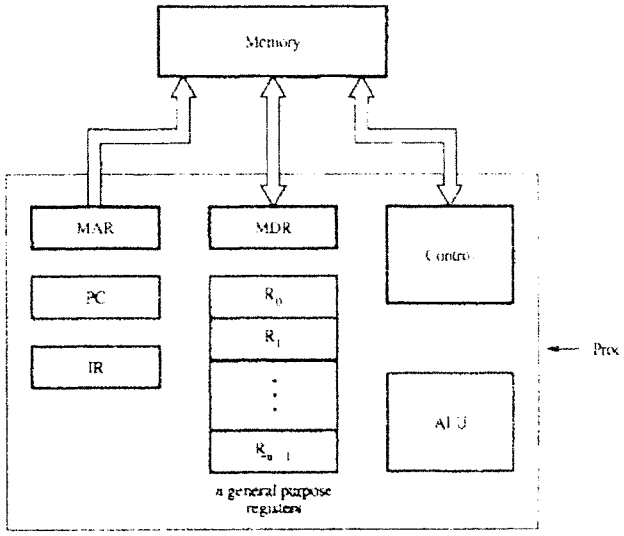


Figure 1.2 Connections between the processor and the memory

Instruction Register It holds the instruction that is currently being executed.

Program Counter: It is another specialized register, which holds the address of next instruction to be fetched and executed.

General Purpose Registers: These registers can be used for temporary storage of data. Processor has 'n' general purpose registers.

MAR & MDR: These two registers provide communication with the memory.

Memory address Register: (MAR) It holds the address of the location to be accessed.

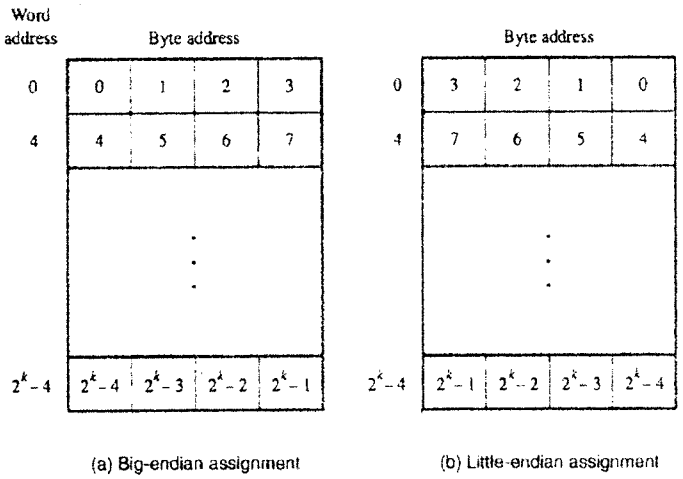
Memory Data Register: It contains the data to be written into or read out of the addressed location.

2

Big Endian and Little Endian Explanation 4 marks

Diagram 6 marks

10 Minutes



	Big-Endian: The name big- endian is used when lower byte addresses are used for the more significant bytes (left most bytes) of the word. Little- Endian: The name little-endian is used for the opposite ordering, where the lower byte addresses are used for the less significant bytes(the right most bytes)of the word.		

Part B (1Q x 10M = 10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question

3	A statement like C = A+B in a high – level language program informs the computer to add the values of the two variables called A and B and assign the sum to a third variable called C. To carry out this kind of operation, assembly language provides three types of instruction formats.
	
	Three address instruction:
	
	• The instruction has the format
	
	operation Source1, source2, Destination
	
	Using this format the above operation can be completed using a single machine instruction as Add A,B,C
	
	This type of instruction has the disadvantage the instruction code will be too large to fit in one word location in memory.
	
	Two address instruction:
	
	• The general format is
	
	operation Source, Destination
	
	An add instruction of this type is Add A,B
	
	• The operation C← [A] +[B] can now be performed by the two – instruction sequence.
	
	Move B,C
	Add A,C
	• But even two address instructions will not normally fit into one word.
	
	One –Address instruction:
		3 Address Instruction 3 marks
		
		2 Address Instruction 3 marks
		
		1 Address Instruction 4 marks
			15 minutes

	• Another possibility is to have machine instructions that specify only one memory operand. When a second operand is needed, as in the case of an add instruction, is understood implicitly to be in a unique location. • A processor register usually called the accumulator may be used for this purpose. • The general format of one address instruction is Operation source/destination e.g. Add A • The operation C ← [A]+[B] can be performed by executing the sequence of instructions. Load A Add B Store C		

Part C (1Q x10 M = 10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
4	a) +2 and +3 0010 + 0011= 0101 No overflow b) -1 and -3 1111+1101=1100 No overflow c) +5 and +6 0101+0110=1011 Overflow d) -4 and -7 1100+1001=0101 Overflow e) -3 and +7 1101+0111=0100 No overflow	Each problem answering correctly 2 marks. 5 X 2= 10 Marks	10 minutes

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BENGALURU

SCHOOL OF ENGINEERING

TEST – 2

Sem & AY: Odd Sem 2019-20
Course Code: CSE 223
Course Name: COMPUTER ORGANIZATION
Program & Sem: B.Tech. (COM/IST/ISE/CCE) & III Sem

Date: 19.11.2019
Time: 11:00 AM to 12:00 PM
Max Marks: 40
Weightage: 20%

Instructions:
(i) *All questions are mandatory.*

Part A[Memory Recall Questions]

Answer the Question. The question carries six marks. **(1Qx6M=6M)**

1. Fill in the blanks by selecting from options provided in brackets.
   a. _____Addressing mode is used in the instruction 'Branch>0 Loop'. **(Index, Relative, Branch, Immediate)** (C.O.NO.2)[Knowledge]
   b. The operation used to remove an element from the stack is called as _____. **(Pop, Push, Insert, Delete)** (C.O.NO.2)[Knowledge]
   c. When subroutine CALL instructions is processed contents of PC is copied to _____register. **(Link, MAR, MDR, IR)** (C.O.NO.2)[Knowledge]
   d. When I/0 devices and the memory share the same address space, the arrangement is called _____ I/0. **(Memory mapped, Interrupt driven, Isolated, DMA)** (C.O.NO.2)[Knowledge]
   e. The routine executed in response to an interrupt request is called as _____. **(Subroutine, Interrupt – Service Routine, Interrupt Function, Interrupt acknowledgement)** (C.O.NO.2)[Knowledge]
   f. _____ are at the top of the memory hierarchy. **(Registers, L1 cache, L2 Cache, Main memory)** (C.O.NO.2)[Knowledge]

Part B [Thought Provoking Questions]

Answer all the Questions. **(3Q=20M)**

2. Explain three possibilities of enabling and disabling interrupts.
   [6M](C.O.NO.2)[Comprehension]

3. Explain stack push and pop operation with instructions using autodecrement mode and autoincrement mode. [4M](C.O.NO.2)[Comprehension]
4. With neat diagram explain internal organization of 32 X 8 memory chip. [10M](C.O.NO.3)[Comprehension]

Part C [Problem Solving Questions]

Answer both the Questions. **(2Q=14M)**

5. Describe following addressing modes with example:
   a. Register b. Immediate c. Base with index
   (C.O.NO.2)[Knowledge]
6. Register R1 and R2 of computer contain the decimal value 1200 and 3800. Identify the addressing mode used and specify the effective address of the source operand in each of the following instructions? (Assume 32 bit word length).
   a. Load 100(R1), R5 b. Store 10(R1,R2), R5
   c. Mov (R2, R5), R4 d. Mov 100,R1
   (C.O.NO.2)[Comprehension]

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

Semester: 3rd

Course Code: CSE223

Course Name: Computer Organization

Date: 19/11/2019

Time: 11:00AM – 12:00PM

Max Marks: 40

Weightage: 20%

Extract of question distribution [outcome wise & level wise]

Q.NO	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels			Thought provoking type [Marks allotted] Bloom's Levels			Problem Solving type [Marks allotted]			Total Marks
			K			C			A			
1	2	Module: 2: Machine Instructions and input/output Units	06									06
2	2	Module: 2: Machine Instructions and input/output Units				06						06
3	2	Module: 2: Machine Instructions and input/output Units				04						04
4	3	Module: 3: Memory System, Basic Processing Unit and Pipelining				10						10
5	2	Module: 2: Machine Instructions and input/output Units				6						6
6	2	Module: 2: Machine Instructions and input/output Units	8									8

	Total Marks											40

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

Annexure- II: Format of Answer Scheme

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

SOLUTION

Semester: 03
Course Code: CSE223
Course Name: Computer Organization

Date: 01/10/2019
Time: 11:00AM:12:00PM
Max Marks: 40
Weightage: 20%

Part A

(6Q x 1M = 06Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	a. Relative b. Pop c. Link d. Memory Mapped e. Interrupt Service Routine f. Registers	Each correct answer 1Marks	9Min

Part B

(1Q x 10M = 10Marks)

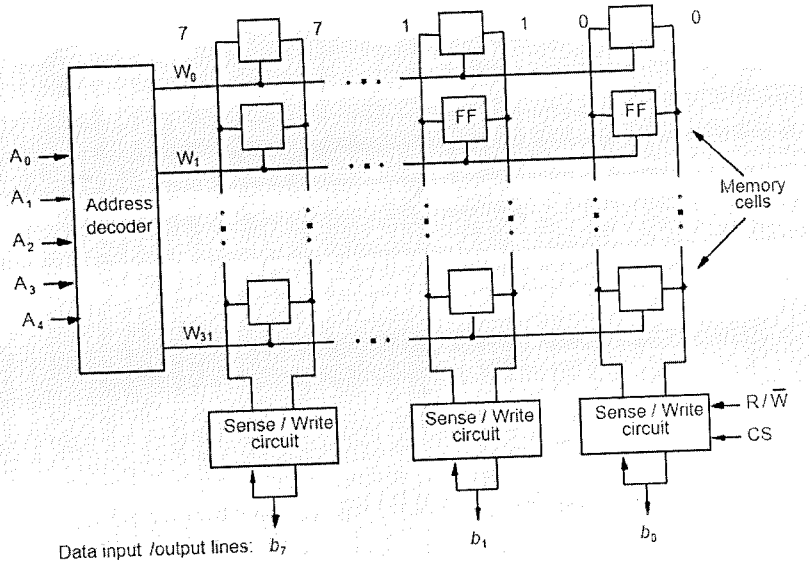
Q No	Solution	Scheme of Marking	Max. Time required for each Question
2	First Possibility: • The processor hardware ignores the interrupt-request line until the execution of the first instruction of interrupt-service routine has been completed. • Then, by using interrupt disable instruction as the first instruction in the interrupt-service routine. • Typically the interrupt-enable instruction will be the last instruction in the interrupt-service routine. Second Possibility: • Using processor status register. • The processor status register has one bit called interrupt-enable which will enable interrupts when set to 1.	Each Possibility 2m 3*2 = 6	10min

	• The processor saves the contents of PC and PROCESSOR STATUS REGISTER(PS) on the stack. • After saving the contents of the PS on the stack, the processor clears the interrupt-enable bit in its PS register, thus disabling further interrupts. • When return from interrupt instruction is executed, the contents of the PS are restored from the stack, setting the interrupt enable bit back to 1, hence interrupts are again enabled. <u>Third Possibility:</u> • The processor has special interrupt request line for which the interrupt-handling circuit responds only to the leading edge of the signal. • Such a line is said to be edge-triggered. • In this case processor will receive only one request, regardless of how long the line is activated. • Hence there is no danger of multiple interruptions and no need to explicitly disable interrupt requests from this line.		

3	If the processor has the autoincrement and autodecrement addressing modes the push operation can be performed by the single instruction
	MOVE NEWITEM, -(SP)
	This instruction moves the word from location NEWITEM onto the top of the STACK decrementing the stack pointer before the move.
	And pop operation can be performed by
	MOVE (SP)+, ITEM
	This instruction moves the top value from the stack into the location ITEM and then increment the stack pointer by 4 so that it points to the new top element.
		Push : 2M
		Pop :2M
			6min

4	• Each memory cell can hold one bit of information. • Memory cells are organized in the form of an array. • One row is one memory word.	**Procedure : 4Marks** **Diagram : 4Marks** **Explanation2M**	**15min**

- All cells of a row are connected to a common line, known as the "word line".
- Word line is connected to the address decoder.
- Sense/write circuits are connected to the data input/output lines of the memory chip.



The figure is an example of a very small memory circuit consisting of 32 words of 8 bits each. This is referred to as a 32 × 8 organization. The data input and the data output of each Sense/Write circuit are connected to a single bidirectional data line that can be connected to the data lines of a computer. Two control lines, R/W and CS, are provided. The R/W Read/Write) input specifies the required operation, and the CS (Chip Select) input selects a given chip in a multichip memory system.

Part C (2Q x 5M =10Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
5	**Register Mode:** The operand is the contents of a processor register, the name(address) of the register is given in the instruction. e.g. MOV R1,R2 The instruction copies the contents of register R1 to register R2.	Each Mode 2Marks	10min

	Immediate mode: • The operand is given explicitly in the instruction. e.g. **MOV 200$_{immediate}$,R0** • The instruction places the value 200 in the register R0. • The immediate mode is used to specify the value of ONLY a source operand. Using a subscript to denote the immediate mode is not appropriate in assembly languages. • A common convention is to use the sharp sign (#) in front of the value to indicate that this value is to be used as an immediate operand. Hence we write the instruction above in the form **MOV #200,R0** **Base with Index:** In this addressing mode Effective Address is the sum of two registers. Syntax: **(R_i,R_j)** Effective Address: **EA= [R_i]+[R_j]** The first register is called Index Register. The second register is called Base Register.		
6	a. Index Mode Effective Address: 100+[R1] = 100+1200=1300 b. Base with Index and Offset Effective Address: 10+[R1]+[R2] = 10+1200+3800=5010 c. Base withIndex Effective Address: [R1]+[R2] =1200 + 3800=5000 d. Immediate: 100 moved to register R1	Mode Specification :1M Effective Address calculations 1 (2*4=8M)	10min

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SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Semester: Odd Semester: 2019 - 20
Course Code: CSE 223
Course Name: COMPUTER ORGANIZATION
Program & Sem: B.Tech (CCE,COM,ISE,IST) & III

Date: 27 December 2019
Time: 1.00 PM to 4.00 PM
Max Marks: 80
Weightage: 40%

Instructions:
(i) Read the questions carefully and answer accordingly.

Part A [Memory Recall Questions]

Answer any two Questions. Each Question carries 12 marks. (2Qx12M=24M)

1. a) Describe the functional units of a computer (C.O.No.1) [Knowledge]

   b) Discuss the following addressing modes with an example

   i) Immediate Addressing Mode

   ii) Indirect Addressing Mode

   iii) Relative Addressing Mode (C.O.No.2) [Comprehension]

2. a) With a neat diagram explain memory hierarchy (C.O.No.3) [Comprehension]

   b) With a neat diagram describe the single bus organization of the data path inside the CPU (C.O.No.3) [Knowledge]

3. a) Discuss 4 bit ripple carry adder hierarchy (C.O.No.4) [Comprehension]

   b) Explain the control sequence for execution of the instruction ADD (R3), (R1) (C.O.No.3) [Comprehension]

Part B [Thought Provoking Questions]

Answer any four Questions. Each Question carries 10 marks. (4Qx10M=40M)

4. With a neat diagram describe the connections between processor and memory (C.O.No.1) [Knowledge]

5. a) Discuss the three possibilities of Enabling and Disabling Interrupts (C.O.No.2) [Comprehension]

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

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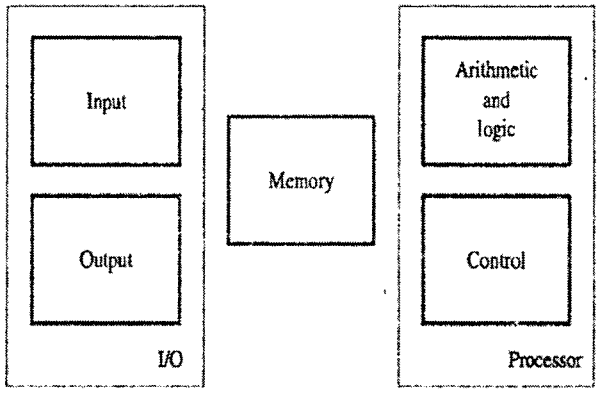
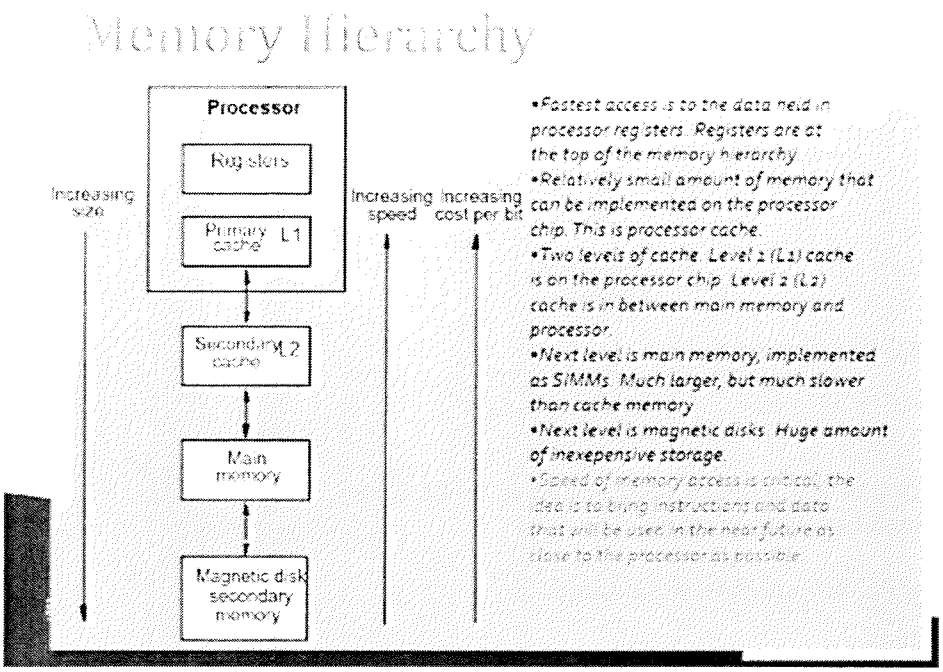
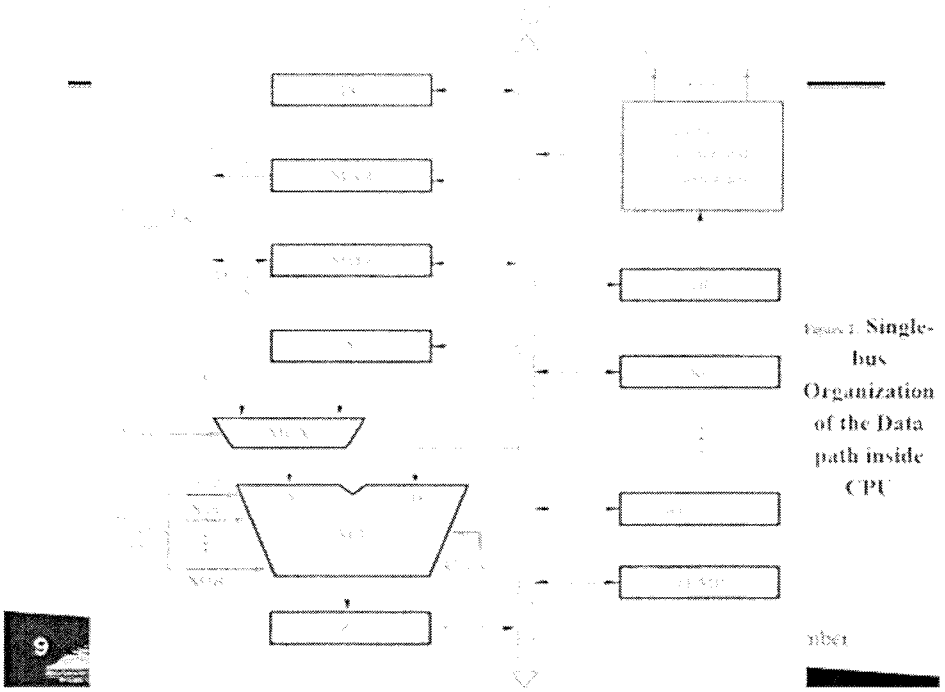
END TERM FINAL EXAMINATION

Extract of question distribution [outcome wise & level wise]

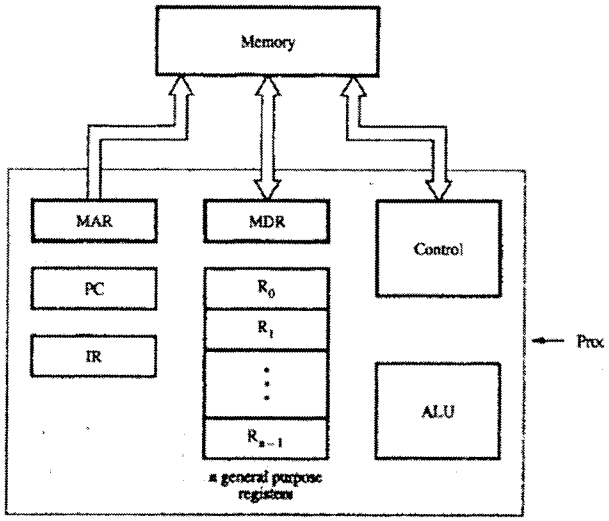
Q.NO.	C.O.NO (% age of CO)	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	A	
PART A Q. NO1	CO1, CO2	Module 1, Module 2	6	6		12
PART A Q. NO 2	CO3	Module 3	6	6		12
PART A Q. NO 3	CO3, CO4	Module 3, Module 4		12		12
PART B Q. NO 4	CO1	Module 1	10			10
PART B Q. NO 5	CO2	Module 2		10		10
PART B Q. NO 6	CO3	Module 3		10		10
PART B Q. NO 7	CO3	Module 3		10		10
PART B Q. NO 8	CO2	Module 2		10		10
PART B Q. NO	CO4	Module 4		10		10

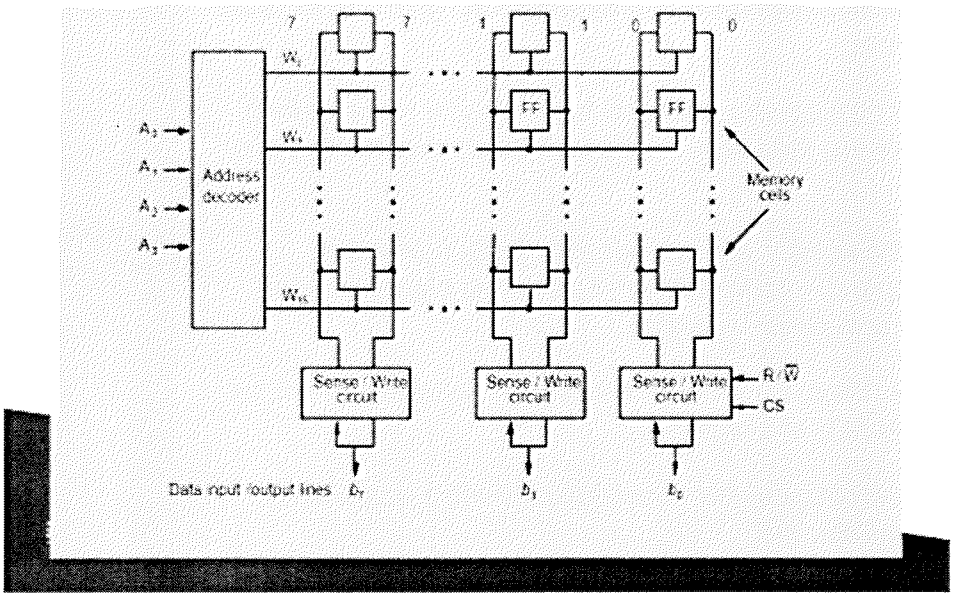
			Question
1 a.	 **Figure 1.1** Basic functional units of a computer. The input unit accepts coded information from users The information received is either stored in the computer's memory or immediately executed by the ALU. The most well-known input device is the key-board. The output unit is the counterpart of the input unit. Its function is to send processed results to the outside world. Storage devices are used to keep data when the power to the computer is turned off. Different forms Hard disk Floppy or zip disks CD-Writer The function of memory unit is to store the programs and data. There are two classes of storage 1) Primary Storage 2) Secondary storage ALU performs the arithmetic operations such as addition, subtraction, multiplication, division and logic operations such as AND, OR, Not. The memory unit, arithmetic and logic and input and output units store and process information and perform input and output operations. The operation of these units must be coordinated in some way. Control unit coordinates and controls the activities among the functional units.	Diagram 2 Marks Explanation 4 Marks	25 Mins
1b.	***Immediate mode:*** • The operand is given explicitly in the instruction. e.g. MOV 200immediate,R0 • The instruction places the value 200 in the register R0. • The immediate mode is only used to specify the value of a source operand. Using a subscript to denote the immediate mode is not appropriate in assembly languages. • A common convention is to use the sharp sign (#) in front of	Each addressing mode 2 marks 3*2=6 M	

2 a		Diagram 3 Marks Explanation 3 Marks	25 Mins
b	 ALU and all the registers are interconnected via a single common bus. The data and address lines of the external memory bus connected to the internal processor bus via the memory data register, MDR, and the memory address register, MAR respectively. Register MDR has two inputs and two outputs. Data may be loaded into MDR either from the memory bus or from the internal processor bus. The data stored in MDR may be placed on either bus. The input of MAR is connected to the internal bus, and its output is connected to the external bus.	Diagram 4M Explanation 2 M	

	phase. • The contents of register R3 are transferred to MAR in step 4, and a memory read operation is initiated. • Then the contents of R1 are transferred to register Y in step 5, to prepare for the addition operation. • When the read operation is completed, the memory operand is available in register MDR, and the addition operation is performed in step 6. • The addition is performed by ALU and the sum is stored in register Z, and then transferred to R1 in step 7. The END signal causes a new instruction fetch cycle to begin by returning to step 1.		

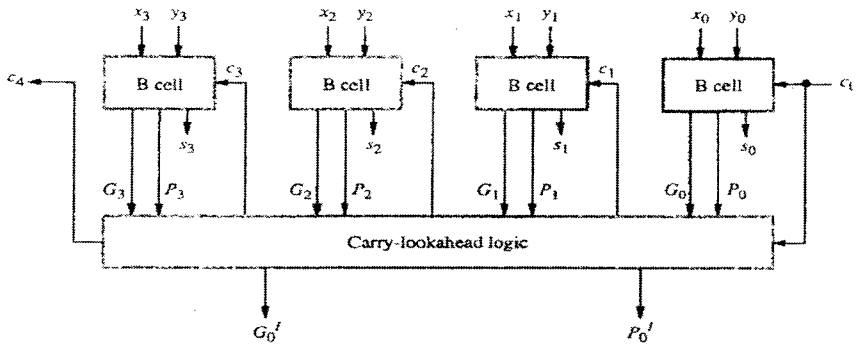
Part B (4Q x 10M = 40 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
4	To perform a given task, an appropriate program consisting of a list of instructions is stored in the memory.  Figure 1.2 Connections between the processor and the memory. Instruction Register It holds the instruction that is currently being executed. Program Counter: It is another specialized register, which holds the address of next instruction to be fetched and executed. General Purpose Registers: These registers can be used for temporary storage of data. Processor has 'n' general purpose registers. MAR & MDR: These two registers provide communication with the memory. Memory address Register: (MAR) It holds the address of the location to be accessed. Memory Data Register: It contains the data to be written into or read out of the addressed location.	Diagram 5 marks 5 registers one mark each	20 Mins

	used. In a pop operation the element on top of the stack is removed. . Since the stack grows in direction of decreasing memory addresses, this means removing the element and then incrementing the stack pointer. However autodecrement mode first decrements the address and then removes the element therefore autodecrement mode cannot be used.		
6	• Each memory cell can hold one bit of information. • Memory cells are organized in the form of an array. • One row is one memory word. • All cells of a row are connected to a common line, known as the "word line". • Word line is connected to the address decoder. Sense/write circuits are connected to the data input/output lines of the memorychip Internal organization of 16 x 8 memory chip  The data input and the data output of each Sense/Write circuit are connected to a single bidirectional data line that can be connected to the data lines of a computer. Two control lines, R/W and CS, are provided. The R/W Read/Write) input specifies the required operation, and the CS (Chip Select) input selects a given chip in a multichip memory system. The memory circuit stores 128 bits and requires 14 external connections for address, data, and control lines. It also needs two	Diagram 5 marks Explanation 5 marks	20 M

	unmodified to bus C. We will call the ALU control signals for such an operation R=A or R=B. • Another feature in figure 7 is the introduction of the **Incrementer unit**, which is used to increment the PC by 4. • Using the Incrementer eliminates the need to add 4 to the PC using the main ALU. The source for the constant 4 at the ALU input multiplexer is still useful. It can be used to increment other addresses such as the memory addresses in load multiple and store multiple instructions.		

8	A statement like C = A+B in a high – level language program informs the computer to add the values of the two variables called A and B and assign the sum to a third variable called C. To carry out this kind of operation, assembly language provides three types of instruction formats.
	<u>Three address instruction:</u>
	• The instruction has the format
	operation Source1, source2, Destination
	Using this format the above operation can be completed using a single machine instruction as Add A,B,C
	This type of instruction has the disadvantage the instruction code will be too large to fit in one word location in memory.
	<u>Two address instruction:</u>
	• The general format is
	operation Source, Destination
	An add instruction of this type is Add A,B
	• The operation C← [A] +[B] can now be performed by the two – instruction sequence.
	Move B,C
	Add A,C
	• But even two address instructions will not normally fit into one word.
	<u>One –Address instruction:</u>
	• Another possibility is to have machine instructions that specify only one memory operand. When a second operand is needed, as in the case of an add instruction, is understood implicitly to be in a unique location.
	• A processor register usually called the accumulator may be used for this purpose.
	• The general format of one address instruction is
		3 Address Instruction 3 marks
		2 Address Instruction 3 marks
		1 Address Instruction 4 marks
			20 Mins



(b) 4-bit adder

Figure 6.4 4-bit carry-lookahead adder.

Part C (1Q x 16M = 16Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
10 a	• +3 and +4 0011 + 0100= 0111 No overflow • -2 and -4 1110+1100=1010 No overflow • +4 and +7 0100+0111=1011 Overflow • -5 and -6 1011+1010=0101 Overflow	2 marks for each sub problem 2*8=16 Marks	30 Mins
b	R5=2020 R6= 3020 32 bit word length i) Load 80(R5), R7 Effective Address: 2100 ii) Move #4000, R7 Effective Address: It is immediate addressing mode. The operand is explicitly mentioned in the instruction itself iii) Subtract – (R5), R7 Effective Address: 2016 iv) Add (R6) +, R7 Effective Address: 3020		

ii)