Roll No.													

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST 1

Sem & AY: Odd Sem. 2019-20 | **Date**: 27.09.2019

Course Code: ECE 201 | **Time**: 2:30PM to 3:30PM

Course Name: ANALOG ELECTRONICS | **Max Marks**: 40

Program & Sem: B.Tech, (ECE/EEE) & III | **Weightage**: 20%

Instructions:

(i) Read the question properly and answer accordingly.

(ii) Question paper consists of 3 parts.

(iii) Scientific and Non-programmable calculators are permitted

---

Part A [Memory Recall Questions]

Answer all the Questions. Each Question carries four marks. (3Qx4M=12M)

1. Define mass action law. Show how current density is related to conductivity and Electric field. (C.O.NO.1) [Knowledge]

2. What is Fermi energy level? Describe how the Fermi level changes with respect to P- type and N-type semiconductor. (C.O.NO.1) [Knowledge]

3. Name the circuit as shown in fig 1 and describe the same with input and output Waveforms. (C.O.NO.1) [Knowledge]

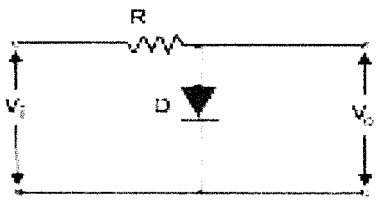


Fig 1

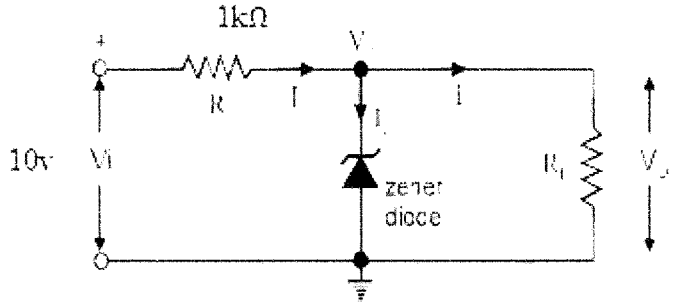
Part B [Thought Provoking Questions]

Answer both the Questions. Each Question carries eight marks. (2Qx8M=16M)

4. a) Find the output voltage for the regulator circuit. Also find I_Z.

(i) R_L=100Ω (ii) R_L=9kΩ.Given V_Z=6v [5M]

(C.O.NO.1) [Comprehension]



b) Distinguish between Zener and Avalanche Breakdown. [3M]

(C.O.NO.1) [Comprehension]

5. A semiconductors hole mobility =200cm^2/v-s and electron mobility=800cm^2/v-s.An Electric field is 10^{14}/cm^3 and hole concentration is 10^{15}/cm^3.The electron concentration Decrease linearly from 10^{14}/cm^3 to 5x10^{13}/cm^3 and that for hole is from 5x10^{15}/cm^3 to 10^{14}/cm^3 over a distance 10cm.area=0.20cm^2.Find total current due to

(i) Electrons (ii) Holes [8M]

(C.O.NO.1) [Comprehension]

Part C [Problem Solving Questions]

Answer the Questions. The Question carries equal marks. (1Qx12M=12M)

6. a) The input of the transistor is Base and output of the transistor is collector identify the transistor configuration explain with a neat circuit diagram and input, output Characteristics. [8M]

(C.O.NO.2) [Comprehension]

b) In a common base I_E=1mA.If emitter circuit is open, collector current is 50μA, α=0.92.Find (i) Total current (ii) β (ii) γ [4M]

(C.O.NO.2) [Comprehension]

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

Semester: III

Course Code: ECE 201

Course Name: Analog Electronics

Date: 27th Sep 2019

Time: 1 Hour

Max Marks: 40

Weightage: 20%

Extract of question distribution [outcome wise & level wise]

Q.NO	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels			Thought provoking type [Marks allotted] Bloom's Levels			Problem Solving type [Marks allotted]			Total Marks
			K			C			C			
1	C.O.1	Module1	4M	k	-	-	-	-	-	-	-	4
2	C.O.1	Module1	4M	k	-	-	-	-	-	-	-	4
3	C.O.1	Module1	4M	k	-	-	-	-	-	-	-	4
4	C.O.1	Module1	-	-	-	8M	C	-	-	-	-	8
5	C.O.1	Module1	-	-	-	8M	C	-	-	-	-	8
6	C.O.2	Module2	-	-	-	-	-	-	12 M	C	-	12
	Total Marks		12			16			12			40

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

[I hereby certify that All the questions are set as per the above guide lines. Ms. Nanditha H G]

Reviewers' Comments

Uneven distribution of time required to solve and marks assigned in all three parts (A, B & C).

Annexure- II: Format of Answer Scheme

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

SCHOOL OF ENGINEERING

SOLUTION

Semester: III

Course Code: ECE201

Course Name: Analog Electronics

Date: 27th Sep 2019

Time: 1 Hour

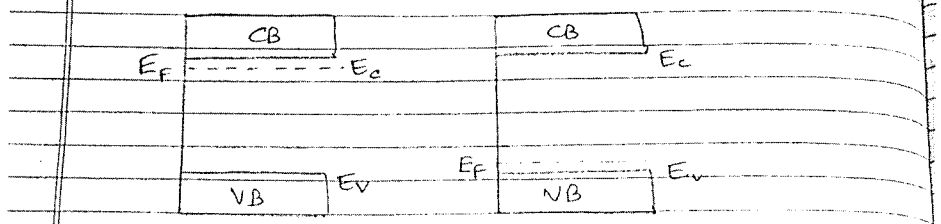
Max Marks: 40

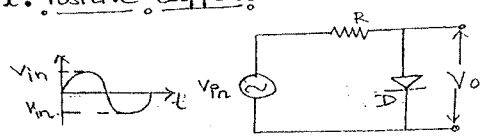
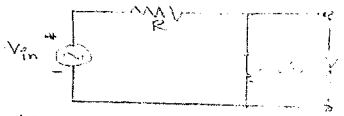
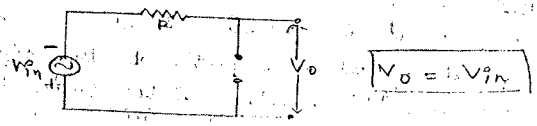
Weightage: 20%

Part A (3x 4 =12 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question

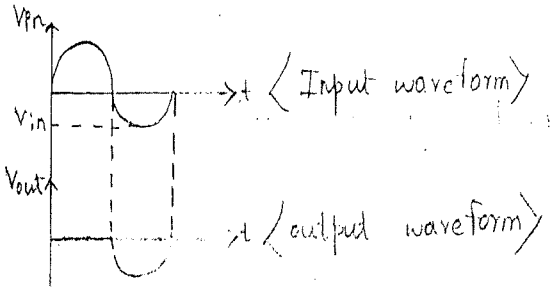
1	**Mass - Action law :-** $n \cdot p = n_i^2$ where $n \rightarrow$ no. of electrons $p \rightarrow$ no. of holes $n_i \rightarrow$ Intrinsic carrier concentration $= 1.45 \times 10^{10}/cm^3$	2	7
	Current Density :-  $I = \frac{q}{t}$ If 'N' e^- are present :- $I = \frac{Nq}{t}$ ... (1) Work to V (cm/s) or (m/s) $V = \frac{l}{t} \Leftrightarrow t = \frac{l}{V}$ Sub t in eqn (1) now $\Rightarrow$ $J = \frac{I}{A} = \frac{NqV}{lA}$ $= qV\left(\frac{N}{Al}\right)$ where $A \rightarrow cm^2$, $l \rightarrow cm$, $\Rightarrow cm^3$ $J = qVn$ $\quad n = \frac{N}{cm^3}$ ↑ concentration $\langle V = \mu E \rangle$ $J = nq\mu E$ $\langle$ from conductivity $\sigma = nq\mu \rangle$ $\boxed{J = \sigma E}$ $\therefore J = \sigma E$ is the expression of current	2	8

2	**Fermi level** It is an imaginary line b/w valence band and conduction band at which will indicate the $\bar{e}$ concentration at a given temp.  • For n-type large no. of electrons will be available in conduction band, so fermi level will lie near conduction band. • Illy for p-type it will lie near valence band because of availability of electons.	4	10

3	i. Positive clipper:-  Assuming the diode is ideal i.e $V_D = 0$ then, (a) During the +ve half cycle:-  ★Here the diode direction and the current direction are same so the diode will be in forward bias and it will make a short-circuited path. ★ The voltage across the short-circuited path is zero and the same voltage will appear across the output as it is connected parallel to it so $V_o = 0$. (b) During the -ve half cycle :-  $V_o = V_{in}$	1+1+1+1 =4	10

★Here the diode direction and the current direction are opposite to eachother so the diode will be in reverse bias and it will make an open-circuited path.

★So the Input voltage will directly appear across the output and $V_o = V_{in}$



Case1 V0=0

Case2 V0=Vin

Part B (2 x 8 =16Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
4	a) Step1 open circuit Zener diode and replace with open circuit voltage Voc Step2 Case1 If Voc is less than Vz Zener diode not conducting Iz=0 Case2 If Voc is greater than Vz Zener diode is conducting and replace with Zener voltage R_L=100Ω V_{oc}=10/11 less than Vz=6v Iz=0 RL=9kΩ Voc=9v Voc greater than Vz=6v So Zener diode is conducting and replaced by Zener voltage Vz=6v Is=I_Z+I_L I_Z=3.34 mA 4b Zener breakdown due to electric field, depletion region thin, occurs at voltage 4v Avalanche breakdown due to high reverse voltage, depletion region thick and voltage is 6v	1+2+2 3	7
5	(ii) Holes μ_p = 200 cm²/V-s μ_n = 800 cm²/V-s E = 2×10^3 V/cm³ n = 10^{14}/cm³ p = 10^{15}/cm³ A = 0.02 cm² x = 10cm $\frac{dn}{dx} = \frac{10^{14} - 5\times10^{13}}{10} = 5\times10^{12}$/cm³ $\frac{dp}{dx} = \frac{5\times10^{15} - 10^{14}}{10} = 4.9\times10^{14}$/cm³ $J_{n(total)} = nq\mu_n E + qD_n\frac{dn}{dx}$ $\frac{D_n}{\mu_n} = V_T \Rightarrow D_n = \mu_n \times V_T$ $= 800 \times 0.026$ D_n= 20.8 cm²/s	1+1+2+2+1+1	10

$I = (10^{14} \times 1.6\times10^{-19} \times 800 \times 2\times10^{3} + 1.6\times10^{-19} \times 20.8 \times$

$\times 0.20$

$\boxed{I_{n(tot)} = 5.12\ A}$

$J_{p(tot)} = pq\mu_p E - qD_p\frac{dp}{dx}$

$\frac{D_p}{\mu_p} = V_T$

$\Rightarrow D_p = V_T \times \mu_p$

$= 200 \times 0.026$

$= 5.2\ cm$

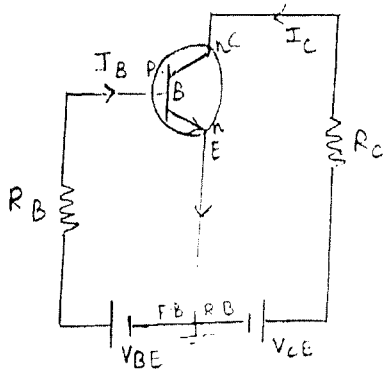
$I_{p(tot)} = (pq\mu_p E - qD_p\frac{dp}{dx}) \times A$

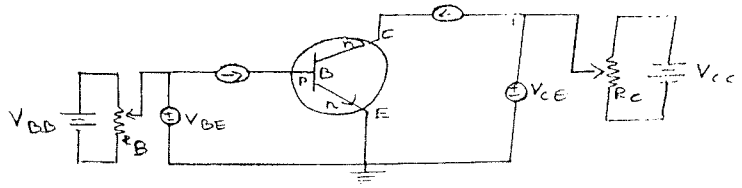
$= (10^{15} \times 1.6\times10^{-19} \times 200 \times 2\times10^{3} - 1.6\times10^{-19} \times 5.2 \times 4.9\times10^{}$

$\times 0.20$

$\boxed{I_{p(tot)} = 12.79\ A}$

Part C (1 x 12 =12 Marks)

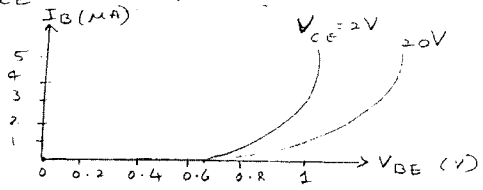
Q No	Solution	Scheme of Marking	Max. Time required for each Question
6a	ii. Common Emitter transistor :- (CE)  ★ Input parameter :- $V_{CE}, I_B, R_B = \frac{}{I_B}$ ★ Output parameter :- $V_{CE}, I_C, R_C = \frac{V}{I_C}$	1+1+1+1 +1+1+2	5



V_{BB} --> base to Ground voltage.
V_{cc} --> collector to Ground voltage.

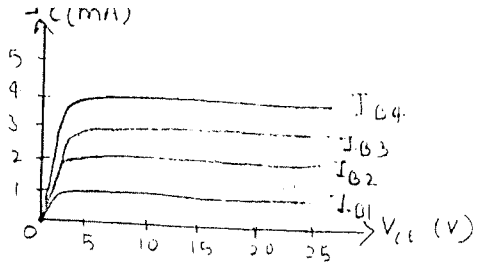
★ Input characteristics:-

This is a graphical relationship b/w input voltag i.e V_{BE} and input current i.e I_B keeping output voltage i.e V_{CE} constant.



★ Output characteristics:-

This is a graphical relationship b/w output voltage and o/p current keeping input current i.e I_B constant.



★ Current gain/amplification factor:-

$$\beta = \frac{\text{O/P current}}{\text{I/P current}} \Rightarrow \beta = \frac{I_C}{I_B} \Rightarrow \boxed{I_C = \beta I_B}$$

★ Expression of output current:-

$$I_C = I_{majority} + I_{minority}$$

$$\boxed{I_C = \beta I_B + I_{CEO}}$$

where, I_{CEO} → Reverse current when input is open.

By comparison,

$$\beta = \frac{\alpha}{1-\alpha} \qquad I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$$

6b	$\beta=\alpha/1-\alpha=11.5$ $\gamma=\beta+1=12.5$	1+1+2	2

	$I_C=\alpha I_E+I_{CBO}=0.970mA$		

Roll No.													

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST – 2

Sem & AY: Odd Sem 2019-20 | **Date**: 16.11.2019

Course Code: ECE 201 | **Time**: 2:30 PM to 3:30 PM

Course Name: ANALOG ELECTRONICS | **Max Marks**: 40

Program & Sem: B.Tech (ECE) & III | **Weightage**: 20%

Instructions:

(i) *Read the question properly and answer accordingly.*

(ii) *Question paper consists of 3 parts.*

(iii) Scientific and Non-programmable calculators are permitted

---

Part A [Memory Recall Questions]

Answer all the Questions. Each Question carries four marks. (3Qx4M=12M)

1. Explain the method of calculating h_{ie} and h_{fe} graphically. (C.O.NO.2) [Knowledge]

2. Answer the following question (C.O.NO.2) [Knowledge]

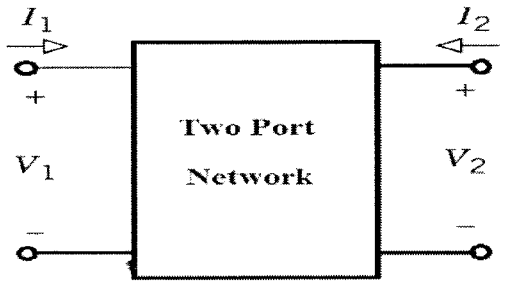


Fig.1

(a) For the above two port network write the equation for hybrid parameters.

(b) Write the h-parameters equation for CE,CC and CB configuration.

3. For a fixed bias circuit given below Vcc=+12V, R_B.= 240 kΩ,R_C.= 5 kΩ, β=50 assume the transistor is Si transistor . Calculate Ic and V_{CE}. (C.O.NO.2) [Comprehension]

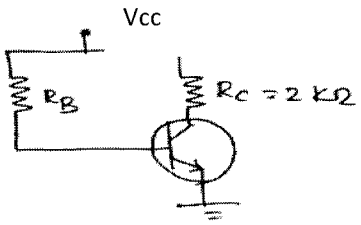


Fig:2

Part B [Thought Provoking Questions]

Answer both the Questions. Each Question carries eight marks. (2Qx8M=16M)

4. Stabilization is determined by a factor called "Stability Factor", derive the same with respect to reverse saturation current (Ico) and voltage between base and emitter

(V_{BE})for emitter bias current. (C.O.NO.2) [Comprehension]

5. Thevini's theorem is applied for reducing the complexity of voltage divider circuit draw the thevinin's equivalent circuit for the voltage divider and calculate thevinin's voltage and resistance, base current and the voltage between collector and emitter.

(C.O.NO.2) [Comprehension]

Given: Vcc= 22 V, β=140, R1=3.9k, R2=3.9k, Rc= 10k , Re= 1.5k

Part C [Problem Solving Question]

Answer the Question. The Question carry twelve marks. (1Qx12M=12M)

6. Derive the following parameters for a transistor amplifier using complete h – parameter model (C.O.NO.2) [Comprehension]

(a) Voltage Gain

(b) Voltage gain including source resistance

(c) Current Gain

(d) Current gain including source resistance

(e) Input impedance

(f) Output admittance

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

Semester: Odd Sem 2019-20
Course Code: ECE 201
Course Name: Analog Electronics

Date: 16/11/19
Time: 2:30pm-3:30 pm
Max Marks: 40
Weightage: 20

Extract of question distribution [outcome wise & level wise]

Q.NO	C.O.NO (%age of CO)	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	A	
1	2	BJT Biasing & Technique	4M	-	-	4M
2	2	BJT Biasing & Technique	4M	-	-	4M
3	2	Small signal Analysis of BJT.	4M	-	-	4M
4	2	BJT Biasing & Technique	-	8M	-	8M
5	2	BJT Biasing & Technique	-	8M	-	8M
6	2	Small signal Analysis of BJT.		12M		12M
	Total Marks		12M	28M		40M

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must

be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

I hereby certify that all the questions are set as per the above guidelines. [Ms. Ishita Deb]

Reviewer's Comments:

(1) Though provoking question requires a descriptive problem statement. Q.4 & Q.5 are not of that type.

(2) Q.5 should be moved to Problem Solving type (A).

(3) Q.6. is also not thought provoking (Q.P. and solution location mismatch)

(4) Part-A - Q.(3) is also Problem Solving type

(5) Unequal distribution of Bloom's level.

12/11/2019

Annexure- II: Format of Answer Scheme

GAIN MORE KNOWLEDGE REACH GREATER HEIGHTS

SCHOOL OF ENGINEERING

SOLUTION

Semester: 3rd

Course Code: ECE 201

Course Name: Analog Electronics

Branch & Sem: ECE & 3rd

Date: 16/11/19

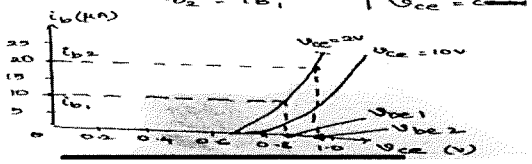
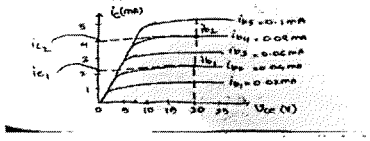
Time: 2.30- 3.30 PM

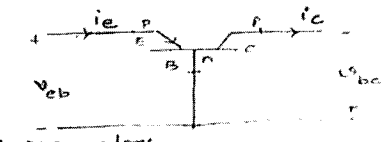
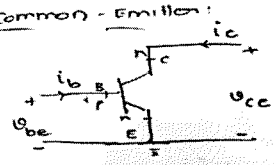
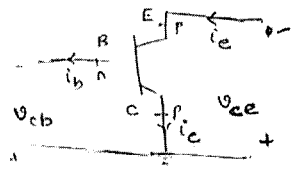
Max Marks: 40

Weightage: 20

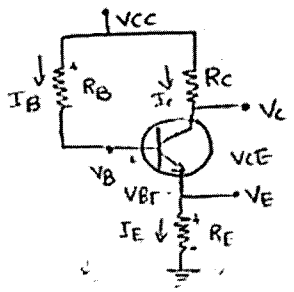
Part A (4Q x 4M = 16Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question

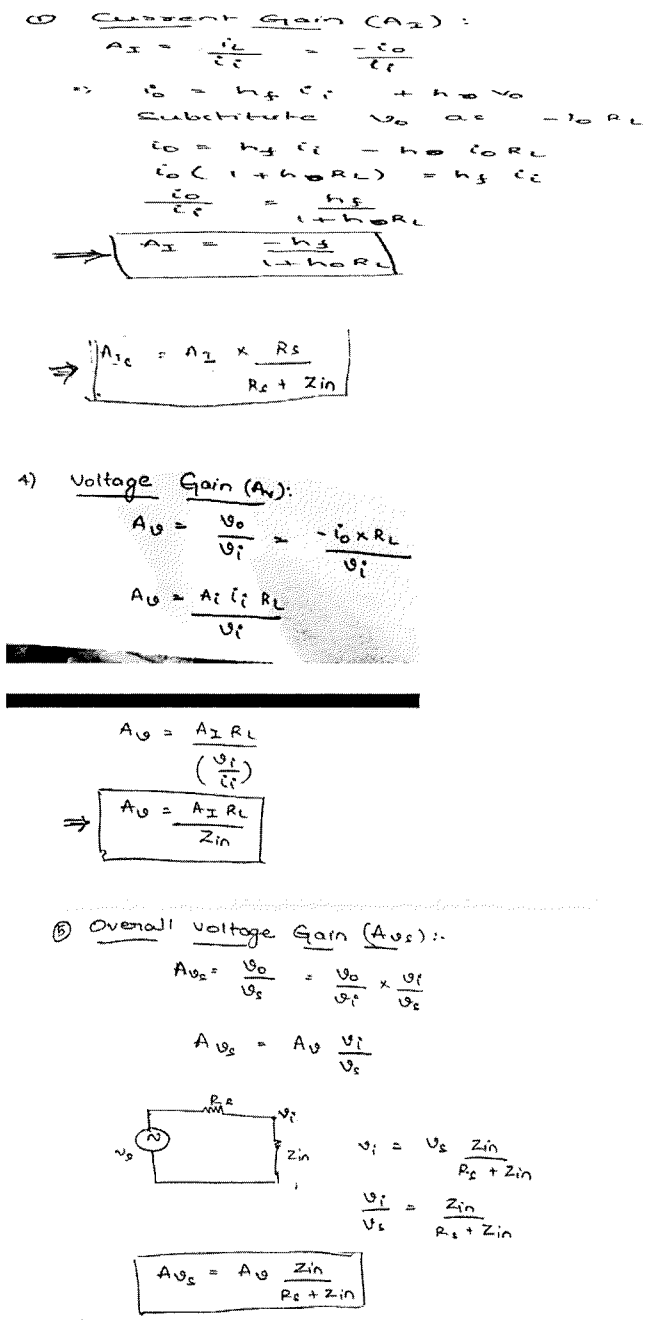
1	$h_{ie} = \frac{v_{be}}{i_b} \Big\vert_{v_{ce}=\text{constant}}$ $= \frac{\Delta v_{be}}{\Delta i_b} \Big\vert_{v_{ce}=\text{constant}}$ $= \frac{v_{be_2} - v_{be_1}}{i_{b_2} - i_{b_1}} \Big\vert_{v_{ce}=2V}$  2. Calculation of h_{fe}: The output characteristics will be drawn between output voltage v_{ce} and output current i_c keeping input current i_b as constant.  $\therefore i_{b_1} = 0.02$ mA $\quad i_{b_2} = 0.04$ mA $i_{b_3} = 0.06$ mA $\quad i_{b_4} = 0.08$ mA $i_{b_5} = 0.1$ mA $h_{fe} = \frac{i_c}{i_b} \Big\vert_{v_{ce}=\text{constant}}$ $= \frac{\Delta i_c}{\Delta i_b} \Big\vert_{v_{ce}=\text{constant}}$ $= \frac{i_{c_2} - i_{c_1}}{i_{b_2} - i_{b_1}} \Big\vert_{v_{ce}=\text{constant}=20V}$ $= \frac{4 - 2.2}{0.08 - 0.04} \Big\vert_{v_{ce}=20V}$ $= \frac{1.8}{0.04} = 45$	**2M- for graph** **2M- Explanation**	**5min**

2	$v_1 = h_{11} i_1 + h_{12} v_2 \quad -①$ $i_2 = h_{21} i_1 + h_{22} v_2 \quad -②$ a) For common-base :  h-parameters $v_{eb} = h_{ib} \cdot i_e + h_{rb} v_{bc} \quad -③$ $i_c = h_{fb} i_e + h_{ob} v_{bc} \quad -④$ b) For Common-Emitter :  $v_{be} = h_{ie} i_b + h_{re} v_{ce} \quad -⑦$ $i_c = h_{fe} i_b + h_{oe} v_{ce} \quad -⑧$ c) common collector  $v_{cb} = h_{ic} i_b + h_{rc} v_{ce} \quad -⑨$ $i_e = h_{fc} i_b + h_{oc} v_{ce} \quad -⑩$	1M- h parameter equation 3M- CE,CC,CB equation	4 min
3	(i) $I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{240} = 0.047$ mA $I_C = \beta I_B = 50 \times 0.047 = 2.35$ mA $I_E = I_B + I_C = 0.047 + 2.35 = 2.397$ mA (ii) $V_{CE} = V_{CC} - I_C R_C = 12 - (2.35)(5 \times 10^{-3})$ $= 12 - 11.75 = 0.25$V	1M- KVL equation 1.5M- VCE 1.5M- IC	5 min

Part B (2Q x 8M = 16 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	 $I_C = \beta I_B + (\beta+1) I_{CO}$ $\Rightarrow I_C = \left\{\frac{V_{CC}-V_{BE}}{R_B+(\beta+1)R_E}\right\}\beta + (\beta+1) I_{CO}$ diff this w.r.t I_C $\frac{dI_C}{I_C} = \left\{\frac{dV_{CC}}{d(R_B+(\beta+1)R_E)} - \frac{dV_{BE}}{d(R_B+(\beta+1)R_E)}\right\} + \frac{d(\beta+1)I_{CO}}{dI_{CO}}$ $\frac{dI_C}{I_C} = \left\{\frac{0-1}{R_B+(\beta+1)R_E}(0-0)\right\} + \frac{dI_{CO}}{dI_C}(\beta+1)$ $\frac{dI_C}{I_C} = \frac{dI_{CO}}{dI_C}(\beta+1)$ $1 = (\beta+1)\frac{1}{S} \Rightarrow S = \frac{1}{\beta+1}$ S' $\frac{dI_C}{dV_{BE}}$ $I_C = \beta I_B + (\beta+1) I_{CO}$ $I_C = \beta\left\{\frac{V_{CC}-V_{BE}}{R_B+(\beta+1)R_E}\right\} + (\beta+1) I_{CO}$ diff w.r.t V_{BE} $\frac{dI_C}{dV_{BE}} = \frac{\beta}{R_B+(\beta+1)R_E}\left\{\frac{dV_{CC}}{dV_{BE}} - \frac{dV_{BE}}{dV_{BE}}\right\} + (\beta+1)\frac{dI_{CO}}{dV_{BE}}$ $\frac{dI_C}{dV_{BE}} = \frac{\beta}{R_B+(\beta+1)R_E}(0-1) + (\beta+1)(0)$ $\boxed{S' = \frac{-\beta}{R_B+(\beta+1)R_E}}$	4+4M	10 min
5.	$V_B = \frac{R_2 V_{CC}}{R_1+R_2} = \frac{3.9\times22}{3.9\times39} = 2V$, $R_B = \frac{R_1R_2}{R_1+R_2} = \frac{39\times3.9}{39+3.9} = 3.6K$. $I_B = \frac{V_B-V_{BE}}{R_B+(\beta+1)R_E} = \frac{2-0.1}{3.5+((41)\times1.5} = 0.006mA$ $I_C = \beta I_B = 140\,(0.006)$ $= 0.84mA$ $V_{CE} = V_{CC} - I_C(R_C+R_E) = 22 - 0.84(11.5) = 12.34V$ $V_C = V_{CC} - I_C R_C = 22 - 0.84\,(10) = 13.6V$ $V_E = V_{CC} - I_C R_E = 22 + 0.84(1.5) = 1.96V$	1M each for equation(1M*4) 1M each for answer (1M*4)	10 min

Part C (1Q x 8M =8 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
7		1M – h parameter equation 2M- equivalent circuit 1.5M for each derivation=9M	15 min

From Eq. (8.28), it is clear that when $A_s \to \infty$, $A_v \to \infty$, $A_i \to \infty$. Therefore, A_i is the current gain of the current source.

2. **Input impedance (Z_i):** The input impedance Z_i is defined as the impedance seen looking into the terminals A–A' of the amplifier. It is given by

$$Z_i = \frac{V_i}{I_i}$$

Applying Kirchhoff's voltage law to the input section of the amplifier we get

$$V_i = h_i I_i + h_r V_o$$

Substituting the value of V_i given by Eq. (8.30) in Eq. (8.29), we get

$$Z_i = \frac{h_i I_i + h_r V_o}{I_i}$$

The output voltage V_o is given by

$$V_o = -I_o R_L = A_i I_i R_L$$

Substituting the value of V_o in Eq. (8.31), we get

$$Z_i = \frac{h_i I_i + h_r A_i I_i R_L}{I_i} = h_i + h_r A_i R_L$$

Substituting the value of A_i given in Eq. (8.25) in the above equation we get

$$Z_i = h_i - \frac{h_r h_f R_L}{1 + h_o R_L}$$

(output admittance (Y_o): The output admittance Y_o is determined by setting the voltage source (V_s) to zero and the ...ent (I_s). The output impedance (Z_o) is determined by setting the voltage source (V_s) to zero and the ...ad impedance R_L to infinity and by driving the output terminals from a voltage source (V_o). Z_o is then ...given by the ratio of the applied voltage (V_o) to output current (I_o).

$$Y_o = \left.\frac{I_o}{V_o}\right|_{V_s = 0,\ R_L = \infty} \tag{8.38}$$

Substituting the value of I_o from Eq. (8.23) in Eq. (8.38), we get

$$Y_o = h_f \frac{I_i}{V_o} + h_o \tag{8.39}$$

Applying Kirchhoff's voltage law to the input section of the circuit in Figure 8.15, we get

$$V_s - R_s I_i - h_i I_i - h_r V_o = 0 \tag{8.40}$$

As $V_s = 0$, therefore

$$R_s I_i + h_i I_i + h_r V_o = 0 \tag{8.41}$$

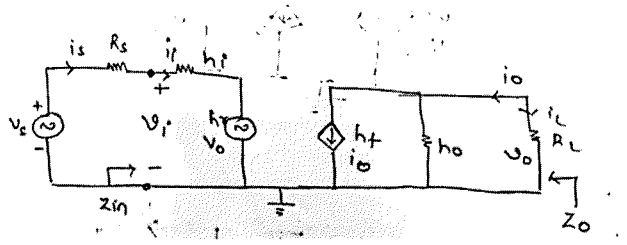
Rearranging the terms in Eq. (8.41), we get

$$\frac{I_i}{V_o} = -\frac{h_r}{h_i + R_s} \tag{8.42}$$

Substituting the value of I_i/V_o given by Eq. (8.42) in Eq. (8.39), we get

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s} \tag{8.43}$$

...ternal to the amplifier. If the effect of load resistor ... of Z_i and R_L.



Roll No.												

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Semester: Odd Semester: 2019-20 | **Date**: 23 December 2019

Course Code: ECE 201 | **Time**: 1:00 PM to 4:00 PM

Course Name: ANALOG ELECTRONICS | **Max Marks**: 80

Program & Sem: B.Tech (ECE & EEE).& III | **Weightage**: 40%

Instructions:

(i) Read the question properly and answer accordingly.

(ii) Question paper consists of 3 parts.

(iii) Scientific and Non-programmable calculators are permitted.

Part A [Memory Recall Questions]

Answer all the sub Questions. Each sub Question carries 2 marks. (10Qx2M=20M)

1.

a. Define Thermal runaway for a transistor. (C.O.No.2) [Knowledge]

b. Write the Barkhausen Criteria For Oscillators. (C.O.No.4) [Knowledge]

c. Cascade structure is used to provide high _____ Gain & Darlington Circuit is used to provide high _____ Gain. (C.O.No.2) [Knowledge]

d. Define Pinch off condition for N-Channel JFET. (C.O.No.3) [Knowledge]

e. Define transconductance (g_m) for N-Channel JFET. (C.O.No.3) [Knowledge]

f. Differentiate between Forward biasing & Reverse Biasing for PN Junction Diode? (C.O.No.1) [Knowledge]

g. If α=0.99, $I_B = 20\mu A$ & $I_{CO} = 10\ nA$, Find Collector Current (I_C). (C.O.No.2) [Knowledge]

h. Mention the efficiencies of Half Wave Rectifier & Full Wave Rectifier? (C.O.No.1) [Knowledge]

i. List two differences between p-type & n-type Semiconductor? (C.O.No.1) [Knowledge]

j. List at least 2 advantages of negative Feedback. (C.O.No.4) [Knowledge]

Part B [Thought Provoking Questions]

Answer all the Questions. Each Question carries 08 marks. (5Qx8M=40M)

2. The feedback circuit where the output voltage is connected in series with the input is called Voltage Series topology. Derive input impedance & output impedance with feedback for this circuit. (C.O.No.4) [Comprehension]

3. For an Emitter Biasing circuit, the following parameters are given: $V_{CC} = 20V, R_B = 430\ K\Omega, R_C = 2\ K\Omega, R_E = 1\ K\Omega, \beta = 50, V_{BE} = 0.7\ V.$ Calculate: $i)\ I_B,\ ii)\ I_C,\ iii)\ V_{CE},\ iv)\ V_C,\ v)\ V_E, vi)\ V_B,\ vii)\ S_{(ICO)},\ viii)\ S_{(Vbe)}$ (C.O.No.2) [Comprehension]

4. The Oscillator which is consisting of LC feedback circuit, with 2 inductors & 1 capacitor is called Hartley Oscillator. Explain the working of this circuit with proper circuit & suitable mathematical expression. (C.O.No.4) [Knowledge]

5. The JFET, where the current is flowing from Drain to source in an n-channel medium with gate are of opposite polarities is called n-channel JFET. Explain the working of the circuit with proper block diagram & input, output characteristics. (C.O.No.3) [Knowledge]

6. Identify the feedback Amplifier which will give high input impedance & high output impedance. For that feedback amplifier, derive input impedance with feedback & output impedance with feedback. (C.O.No.4) [Comprehension]

Part C [Problem Solving Questions]

Answer both the Questions. Each Question carries 10 marks. (2Qx10M=20M)

7.

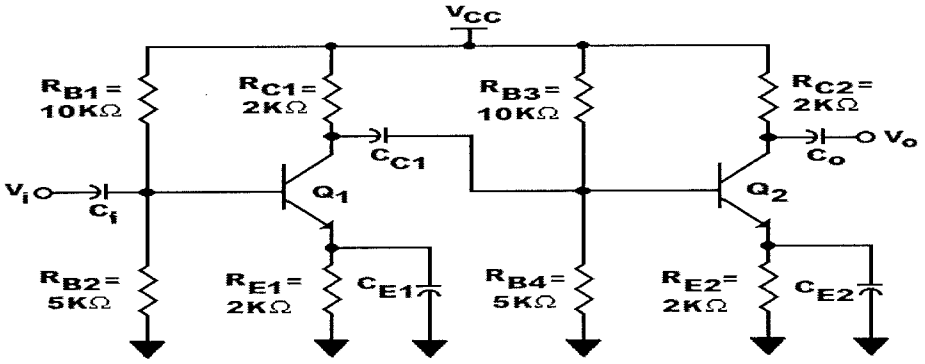
a. Why Darlington transistors are also referred to as super beta transistors? Explain the concept using the internal schematic of Darlington transistors with relevant mathematical expressions by using DC Analysis. [6M]
(C.O.No.2) [Knowledge]

b. Pure silicon has an electrical resistivity of 3000 Ω-m. If the carrier density in it is $1.1 \times 10^6/m^3$ & the electron mobility is three times that of hole mobility, calculate the mobility of electrons & holes. [4M]
(C.O.No.1) [Knowledge]

8.

a. Figure below shows a 2-stage BJT cascaded amplifier. Given h_{ie} = 2 kΩ and h_{fe} = 100. Assume h_{oe} effect negligible. Consider load impedance of second stage is 5KΩ. Vcc= 20V. Calculate: [8M]
(C.O.No.3) [Comprehension]

i) Voltage gain for each stage.
ii) Total Voltage gain.
iii) Total Current gain.



b. Differentiate between BJT & FET. Mention at least 4 points. [2M]
(C.O.No.3)[Knowledge]

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

Semester: Odd Sem 2019-20

Course Code: ECE 201

Course Name: **Analog Electronics**

Date: 23/12/19

Time: 1.00 pm- 4.00 pm

Max Marks: 80

Weightage: 40

Extract of question distribution [outcome wise & level wise]

Q.NO	C.O.NO (%age of CO)	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	A	
1	1,2,3,4	Module 1, 2,3, 4	20M	-	-	20M
2	4	Feedback Amplifier	-	8M	-	8M
3	2	Transistor Biasing	-	8M	-	8M
4	4	Oscillator	8M	-	-	8M
5	3	FET	8M	-	-	8M
6	4	Feedback Amplifier	-	8M	-	8M
7.a	2	Multistage amplifier	6M	-	-	6M
7.b	1	Semiconductor Physics	4M	-		4M
8.a	3	Multistage Amplifier	-	8M	?	8M
8.b	3	FET	2M-			2M
	Total Marks		48M	32M		80M

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

I hereby certify that all the questions are set as per the above guidelines. [Mr. Swastik Sahoo]

Reviewer's Comments: Thought Provoking Questions must be asked as per guidelines, from next Sem. onwards. Qn 8 @ should be in Application Level.

17/12/19

Annexure- II: Format of Answer Scheme

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE REACH GREATER HEIGHTS

SOLUTION

Semester: 3rd

Course Code: ECE 201

Course Name: **Analog Electronics**

Branch & Sem: ECE & 3rd

Date: 23/12/19

Time: 1.00 – 4.00 pm

Max Marks: 80

Weightage: 40

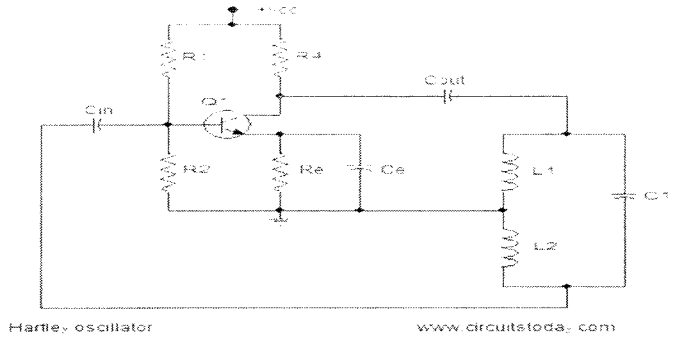
Part A (Q x M = Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	a. Thermal Runaway: Taking CE equation, $I_c = \beta I_B + (\beta + 1)I_{CO}$. If the temp. will increase, then reverse saturation current & Amplification factor will increase. So for a small increase in temp. there will be large variation in collector current & if it will exceed the rated value, the circuit may break down. This is called Thermal Runaway	2	3 Min
	b. Barkhausen Criteria: - The loop gain must be equal to 1. - The total Phase shift must be 0° or 360° .	1M for each	2 Min
	c. Voltage Gain & Current Gain.	1M for each	1 Min
	d. The reverse voltage at which, two depletion region at each side of the gate will touch each other & the flow of current saturates & remains constant. This is called Pinch-Off condition.	2	2 Min
	$e. g_m = \frac{2I_{DSS}}{\lvert V_P \rvert} \times (1 - \frac{V_{GS}}{V_P})$	2	3 Min

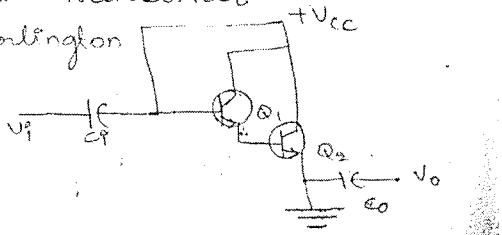
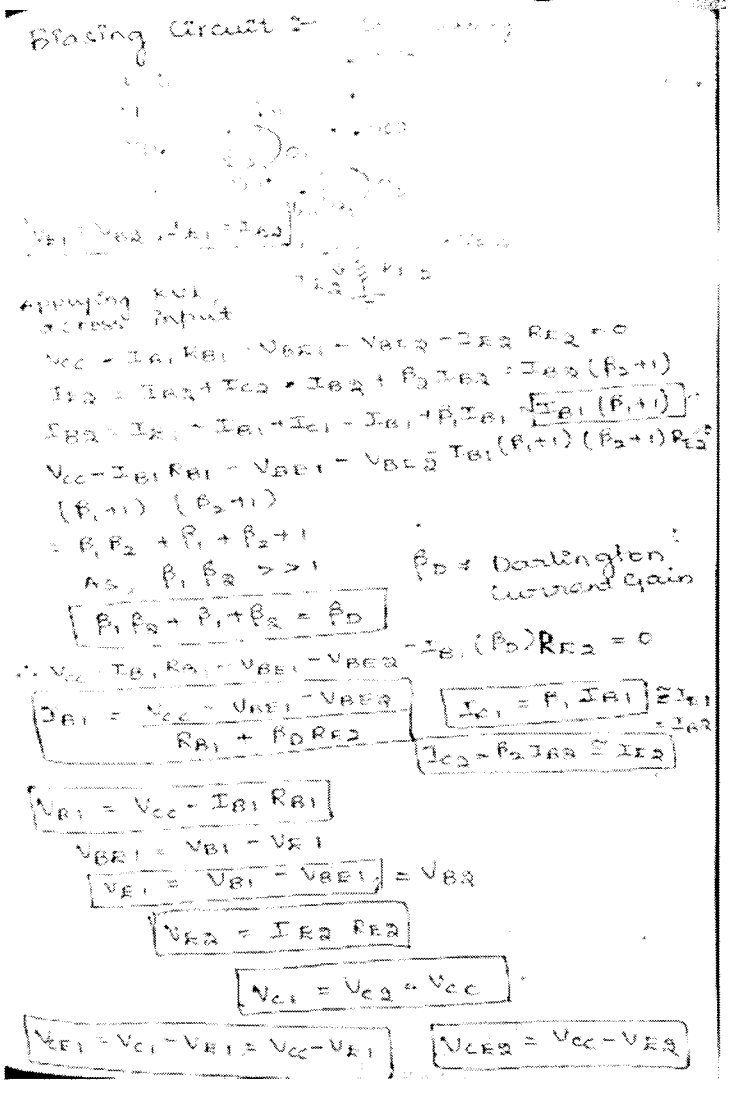
	f. When p-type is connected to positive & n-type is connected to negative, then it is called Forward Biasing & when the connection is reverse, then it is called Reverse Biasing.	**1M for each**	**2 Min**
	g. $I_C = \beta I_B + (\beta + 1)I_{CO}$= 1.98 mA	**2**	**3 Min**
	h. For Half Wave Rectifier: 40.6% & Full Wave Rectifier: 81.2%.	**1M for each**	**2 Min**
	i. P-type: Majority charge carrier is holes & less conductivity. N-type: Majority charge carrier is electron & More Conductivity.	**1M for each**	**3 Min**
	j. Negative Feedback: - More Stable. - Less distortion & less frequency Distortion.	**1M for each**	**3 Min**

Part B (2Q x 8M = 16 Marks)

Q No	**Solution**	**Scheme of Marking**	**Max. Time required for each Question**
2	Voltage Series is called series-shunt, i.e. input is connected in series & output is connected in parallel. Input impedance is given as: $R_{if} = R_i(1 + A\beta)$ & the output impedance is given as$R_{of} = \frac{R_o}{(1+A\beta)}$. Here, A is the forward voltage gain & β is the feedback factor.	2M each for Block Diag. + Circuit Diag. + Input Impedance+ Output Impedance	10
3	$i)\ I_B = \frac{V_{CC} - V_{BE}}{R_B} = 40.1\mu A.$ $ii)\ I_C = \beta I_B = 2.01\ mA$ $iii)\ V_{CE} = V_{CC} - I_C(R_C + R_E) = 13.97\ V.$ $iv)\ V_c = V_{CC} - I_C R_C = 15.98\ V.$ $v) V_E = I_C R_E = 2.01\ V$ $vi)\ V_B = V_{BE} + V_E = 2.71\ V$ $vii)\ S_{(ICO)} = (\beta + 1)\frac{R_B + R_E}{R_B + (\beta + 1)R_E} = 45.69$ $viii) S_{(VBE)} = \frac{-\beta}{R_B + (\beta + 1)R_E} = -0.10\ m\Omega^{-1}$	1M for Each Parameter	10
4	Hartley Oscillator: In a Hartley oscillator, the oscillation frequency is determined by a tank circuit comprising of two inductors and one capacitor. The inductors are connected in series and the capacitor is connected across them in parallel.	3M for Diagram+ 5 M for Working	10

	 When the power supply is switched ON the transistor starts conducting and the collector current increases. As a result the capacitor C1 starts charging and when the capacitor C1 is fully charged it starts discharging through coil L1. This charging and discharging creates a series of damped oscillations in the tank circuit and it is the key. The oscillations produced in the tank circuit is coupled (fed back) to the base of Q1 and it appears in the amplified form across the collector and emitter of the transistor. The output voltage of the transistor (voltage across collector and emitter) will be in phase with the voltage across inductor L1. Since the junction of two inductors is grounded, the voltage across L2 will be 180° out of phase to that of the voltage across L1. The voltage across L2 is actually fed back to the base of Q1. From this we can see that, the feedback voltage is 180° out of phase with the transistor and also the transistor itself will create another 180° phase difference. So the total phase difference between input and output is 360° and it is very important condition for creating sustained oscillations.		
5	N-Channel JFET: JFET stands for Junction Field Effect Transistor. The input circuit is connected in Reverse Biasing & output is in forward biasing. When V_{DS} will be applied the drain current will start to flow from drain to source. If the medium is n-type then it is called n-channel. Gate will be of opposite type, i.e. p-type & at the junction depletion region will be formed. When reverse voltage V_{GS} is applied then the width of the depletion region will increase. If further that voltage will be increased the width of the depletion regions will touch each other & the drain current will stop. That condition is called pinch off condition, The Shockley's equation describing that can be expressed as: $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$	2M construction+ 2M Explanation+ 2M input characteristics +2M Output Chracteristics	10
6	Current Series is called series-series, i.e. input is connected in series & output is connected in series. Input impedance is given as: $R_{if} = R_i(1 + A\beta)$ & the output impedance is given as$R_{of} = R_o(1 + A\beta)$. Here, A is the forward voltage gain & β is the feedback factor.	2M each for Block Diag. + Circuit Diag. + Input Impedance+ Output Impedance	10

Part C (1Q x12 M =12 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
7. a	Darlington Connection :- 1st condition :- Collector of both the transistor will be connected to V_{cc} 2nd :- Emitter of 1st transistor is connected to base of 2nd transistor Layout of Darlington (CE-CC) 2- modes  Biasing Circuit :-  Applying KVL Darlington current gain $\beta_D = \beta_1\beta_2 + \beta_1 + \beta_2 + 1$ $\beta_1\beta_2 + \beta_1 + \beta_2 = \beta_D$ $I_{B1} = \frac{V_{cc} - V_{BE1} - V_{BE2}}{R_{B1} + \beta_D R_{E2}}$ $I_{C1} = \beta_1 I_{B1} \cong I_{E1} = I_{B2}$ $I_{C2} = \beta_2 I_{B2} \cong I_{E2}$ $V_{B1} = V_{cc} - I_{B1} R_{B1}$ $V_{BE1} = V_{B1} - V_{E1}$ $V_{E1} = V_{B1} - V_{BE1} = V_{B2}$ $V_{E2} = I_{E2} R_{E2}$ $V_{C1} = V_{C2} = V_{cc}$ $V_{CE1} = V_{C1} - V_{E1} = V_{cc} - V_{E1}$ $V_{CE2} = V_{cc} - V_{E2}$	2M circuit+ 4M for Derivation	12
7.b	Conductivity is the reciprocal of resistivity. $\sigma = nq(\mu_n + \mu_p)$. Applying this & from the relation, $\mu_n = 3\mu_p$, $\mu_p = 4.7348 \times 10^8 \frac{m^2}{V-Sec}$ & $\mu_n = 1.42 \times 10^9 \frac{m^2}{V-Sec}$	2 M for each parameter	6 Min

8.a	**First Stage:** $R_B = \frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}} = 3.33K\Omega.$ **Input Impedance:** $Z_{in} = \frac{R_B h_{ie}}{R_B+h_{ie}} = 1.24\ K\Omega.$ **Output Impedance:** $Z_{out} = R_C = 2\ K\Omega$ **Voltage Gain=** $-\frac{h_{fe}Z_{out}}{Z_{in}} = -161.29$ **Second Stage:** $R_B = \frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}} = 3.33K\Omega.$ **Input Impedance:** $Z_{in} = \frac{R_B h_{ie}}{R_B+h_{ie}} = 1.24\ K\Omega.$ **Output Impedance:** $Z_{out} = R_C = 2\ K\Omega$ **Voltage Gain=** $-\frac{h_{fe}Z_{out}}{Z_{in}} = -161.29$ **ii) Total Voltage Gain: 26014.46** **iii) Total Current Gain=** $A_{IT} = \frac{A_{VT}R_C}{Z_{in1}} = 104897.01$	4M for the voltage gain of each stage + 2M for total Voltage Gain +2M for total Current Gain	15 Min
b	BJT: Bipolar Junction Transistor, Current Controlled Device, More Switching Time, More Noise along with the symbols & its terminals. FET: Unipolar Junction Transistor, Voltage Controlled Device, Less Switching time, Less Noise along with the symbols & its terminals	0.5 M for each point	10 Min