Roll No.														

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST 1

Sem & AY: Odd Sem. 2019-20
Course Code: ECE 220
Course Name: DIGITAL ELECTRONICS
Program & Sem: BTech (ECE) & III

Date: 30.09.2019
Time: 2:30PM to 3:30 PM
Max Marks: 40
Weightage: 20%

Instructions:

(i) Question paper consists of two pages
(ii) Scientific and Non-programmable calculators are permitted

Part A [Memory Recall Questions]

Answer all the Questions. Each Question carries one marks (12Qx1M=12M)

1 a) The BCD sum of $(4)_{10}$ and $(6)_{10}$ is _____. (C.O.NO.1) [Knowledge]

b) The diminished radix complement of $(135)_{10}$ is _____. (C.O.NO.1) [Knowledge]

c) The gray code of $(1000)_2$ is _____. (C.O.NO.1) [Knowledge]

d) Choosing the signal value high level 'H' to represent logic 1 & low level 'L' to represent logic 0, defines _____ logic system (C.O.NO.1) [Knowledge]

e) The complement of Boolean function F = A'BC' + A'B'C is _____. (C.O.NO.1) [Knowledge]

f) $\overline{x + y}$ = _____. (C.O.NO.1) [Knowledge]

g) $(x + y)(x + \bar{y})$ = _____. (C.O.NO.1) [Knowledge]

h) The excess 3 code of $(2231)_{10}$ is _____. (C.O.NO.1) [Knowledge]

i) BCD code of $(9045)_{10}$ is _____. (C.O.NO.1) [Knowledge]

j) The binary product of $(1010)_2$ and $(1100)_2$ is _____. (C.O.NO.1) [Knowledge]

k) The hexadecimal number system has a base value of _____. (C.O.NO.1) [Knowledge]

l) $(10AB)_{16}$ = (_____)$_{10}$ (C.O.NO.1) [Knowledge]

Part B [Thought Provoking Questions]

Answer all the Questions. Each Question carries four marks. (4Qx4M=16M)

2. Perform the following conversions

   a) $(10110001101011.11110010)_2$ to hexadecimal equivalent. (C.O.NO.1) [Knowledge]
   b) $(673.124)_8$ to binary equivalent. (C.O.NO.1) [Knowledge]

3. Draw the logic diagram corresponding to the following Boolean expression without simplifying it. $F = D + BC + (D + \bar{C})(\bar{A} + C)$ (C.O.NO.1) [Knowledge]

4. Draw the NAND- NAND implementation for the Boolean function $= \bar{x}y + x\bar{y}$. (C.O.NO.1) [Knowledge]

5. a. Differentiate between canonical form and standard form. (C.O.NO.1) [Knowledge]

   b. Develop a truth table for Boolean expression $F = \bar{y} + \bar{x}\bar{z}$. (C.O.NO.1) [Knowledge]

Part C [Problem Solving Questions]

Answer both the Questions. Each Question carries six marks. (2Qx6M=12M)

6. Simplify the Boolean expression using 4 variable k map and obtain SOP expression. Indicate the number of terms and number of literals in the simplified expression.

   $F(w, x, y, z) = \sum(0,1,2,4,5,6,8,9,12,13,14)$. . (C.O.NO.2) [Comprehension]

7. Identify the minterms & maxterms of the truth table for F shown below. Write the sum of minterms and product of maxterms expression. (C.O.NO.1) [Knowledge]

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE REACH GREATER HEIGHTS

Semester: 3RD

Course Code: ECE 220

Course Name: Digital Electronics

Date: 30-09-2019

Time: 2:30 PM – 3:30 PM

Max Marks: 40

Weightage: 20%

Extract of question distribution [outcome wise & level wise]

Q.NO.	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	A	
1 a - l	CO1	MODULE 1	1 MARK EACH (K)			12
2-5	CO1	MODULE 1		4 M EACH (K)		16
6	CO2	MODULE 2			6 M (C)	6
7	CO1	MODULE 1			6 M (K)	6
	Total Marks					40

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

Reviewer's Comments: (1) Part 'C' solution total error (16 marks)
(2) Part 'C' – Qn – 7, solution incomplete (expression missing)

Annexure- II: Format of Answer Scheme

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

SOLUTION

Semester: 3RD
Course Code: ECE 220
Course Name: Digital Electronics
Program & Sem: BTech & 3RD (2018 Batch)

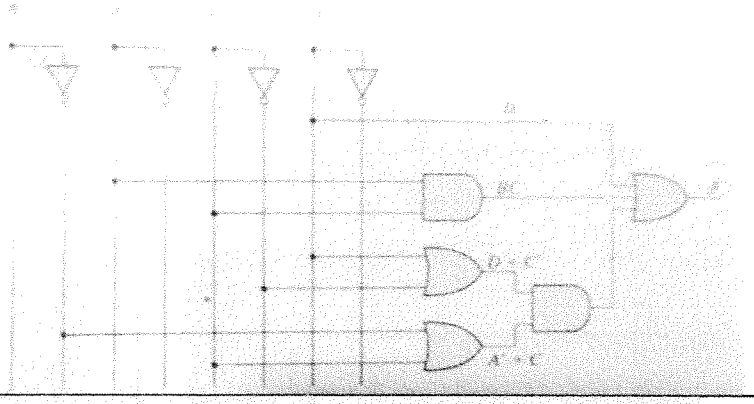
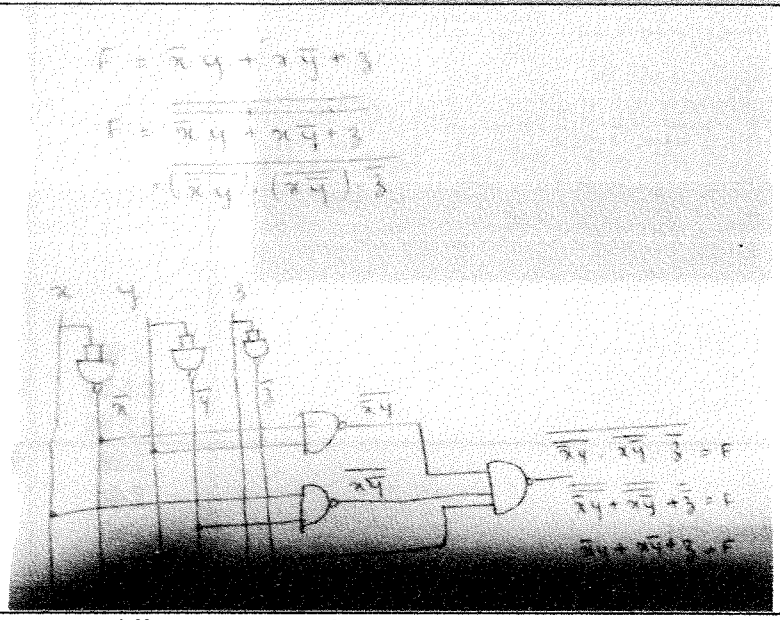
Date: 30-09-2019
Time: 2:30 PM – 3:30 PM
Max Marks: 40
Weightage: 20%

Part A (10Q x 1M = 10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1.a.	$(10000)_{BCD}$	1 mark	1 MINUTE
b	$(864)_{10}$	1 mark	1 MINUTE
c	1100	1 mark	1 MINUTE
d	POSITIVE	1 mark	1 MINUTE
e	$(A + \bar{B} + C)(A + B + \bar{C})$	1 mark	1 MINUTE
f	X'+Y'	1 mark	1 MINUTE
g	X	1 mark	1 MINUTE
h	$(0101010101100100)_{excess\ 3}$	1 mark	1 MINUTE
i	$(1001000001000101)_{BCD}$	1 mark	1 MINUTE
j	$(1111000)_2$	1 mark	1 MINUTE
k	16	1 mark	1 MINUTE
l	$(4267)_{10}$	1 mark	1 MINUTE

Part B

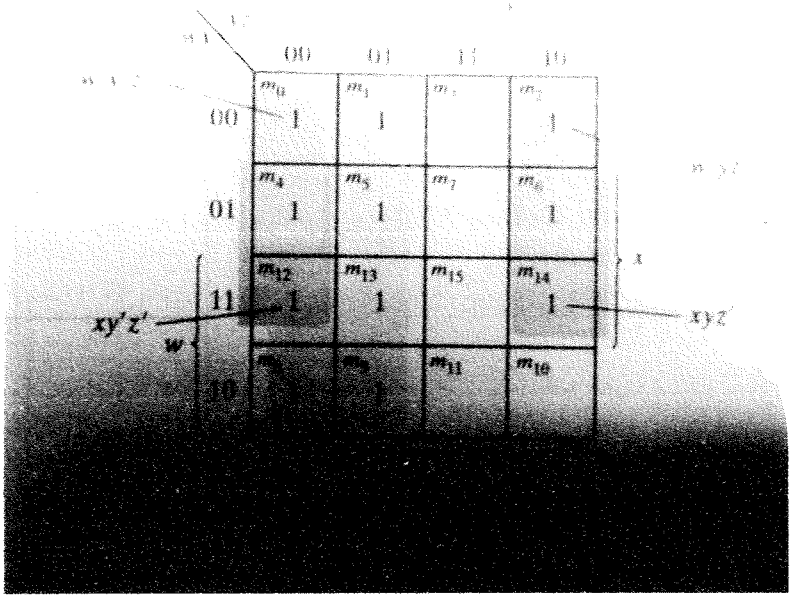
(4Q x 4M = 16 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
2. a	Steps Final answer $(2C6B.F2)_{16}$	1.5 M 0.5 M	4 MINUTES
2.b	Steps Final answer $(110111011.001010100)_2$	1.5 M 0.5 M	4 MINUTES
3		4 M	5 MINUTES
4		0.5 M 0.5 M 3 M	5 MINUTES
5 a	Any two differences 1M each	2 M	5 MINUTES
5 b		2 M	5 MINUTES

x	y	z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1

	1	0	0	1			
	1	0	1	1			
	1	1	0	1			
	1	1	1	0			

Part C (2Q x 6M = 6 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
6		4 M	8 MINUTES
	F= y' + w'z' + xz' Number of terms = 3 Number of literals = 5	1 M 0.5 M 0.5 M	
7	MINTERMS MAXTERMS sum of minterms expression product of maxterms expression	2 M 2 M 1M 1M	8 MINUTES

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GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST –2

Semester	: **III**	**Date**	: **18-11-2019**
Course Code	: **ECE 220**	**Time**	: **2.30 pm-3.30 pm**
Course Name	: **DIGITAL ELECTRONICS**	**Max Marks**	: **40 Marks**
Program & Sem	: **B.Tech (ECE) & III**	**Weightage**	: **20%**

Instructions:

i. Read Questions carefully and answer accordingly
ii. Non-Programmable Scientific Calculators permitted
iii. This question paper contains two pages

Part A
Answer ALL the Questions. Each question carries1 marks. **CO** **(6Qx1M=6M)**

1.

i.	**If A,B and C are the inputs of a full adder then sum is given by _____**	(CO3)	[Knowledge Level]
ii.	**If A, B and C are the inputs of a full adder then the carry is given by_____**	(CO3)	[Knowledge Level]
iii.	**If A and B are the input of a subtractor then the borrow will be_____**	(CO3)	[Knowledge Level]
iv.	**How many select lines would be required for an 8-line-to-1-line multiplexer**	(CO3)	[Knowledge Level]
v.	**The enable input in multiplexer is also known as _____**	(CO3)	[Knowledge Level]
vi.	**A magnitude comparator is defined as a digital comparator which has _____ number of output terminal.**	(CO3)	[Knowledge Level]

Part B

Answer all the Questions. Each question carries 8 marks. **CO** **(3Qx8M=24M)**

2.	**Design a combinational circuit using ExOR gates which has 4 bit Binary input and 4 bit Gray Code output representations**	(CO3)	[Comprehension Level]
3.	**Design Full Adder using two Half Adder and OR gate**	(CO3)	[Comprehension Level]
4.	**Implement the given function using 8x1 MUX F(M,N,O,P)=$\sum m\,(0,2,3,6,8,9,13,14)$**	(CO3)	[Comprehension Level]

Part C

Answer *ALL* the Questions. Each question carries 10 marks. **CO** **(1Qx10M=10M)**

5.	**Find all the prime implicants of the function given below F(A,B,C,D)= $\sum m\,(0,1,3,7,8,9,11,15)$ using Quine-McCluskey tabular method.**	(CO2)	[Comprehension Level]

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST – 2

Semester	**: III**	**Date**	**: 18-11-2019**
Course Code	**: ECE 220**	**Time**	**: 2.30 pm-3.30 pm**
Course Name	**: DIGITAL ELECTRONICS**	**Max Marks**	**: 40 Marks**
Program & Sem	**: B.Tech (ECE) & III**	**Weightage**	**: 20%**

Extract of question distribution [outcome wise & level wise]

Q.NO.	C.O. NO.	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	A	
1	3	Module3	6x1			6marks
2	3	Module3		8		8marks
3	3	Module3		8		8Marks
4	3	Module3		8		8marks
5	2	Module2		10		10marks
	Total Marks		6	34		40 marks

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60% Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

Reviewer's Comments :-

1) No thought provoking question given.
2) Q.5, consider as problem solving.
3) Similarly, no application level
4) No equal distribution for Bloom's level

12/11/19

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST – 2

Semester	**: III**	**Date**	**: 18-11-2019**
Course Code	**: ECE 220**	**Time**	**: 2.30 pm-3.30 pm**
Course Name	**: DIGITAL ELECTRONICS**	**Max Marks**	**: 40 Marks**
Program & Sem	**: B.Tech (ECE) & III**	**Weightage**	**: 20%**

Part A **(6Q x 1M = 6Marks)**

Q. No.	Solution	Scheme of Marking	Max. Time required for each Question
1	i. A XOR B XOR C	1	1min
	ii. (A AND B) OR (B AND C) OR (C AND A)	1	1min
	iii. A' AND B	1	1min
	iv. Three	1	1min
	v. Strobe	1	1min
	vi. Three	1	1min

Part B **(3Q x 8M = 24 Marks)**

Q. No	Solution	Scheme of Marking	Max. Time required for each Question
2	**Binary to Gray Code Converter:**	Truth table=2M + K-Map=4M + Logic Diagram=2M	10 min

Binary				Gray Code			
b_3	b_2	b_1	b_0	g_3	g_2	g_1	g_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

For g0 :

b3,b2 \ b1,b0	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

For g1:

b3.b2 \ b1,b0	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1

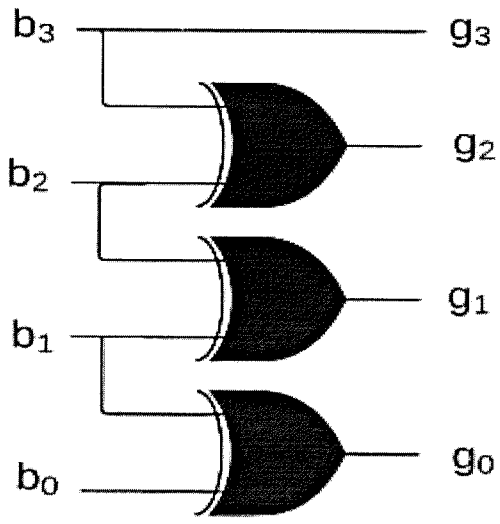
For g2 :

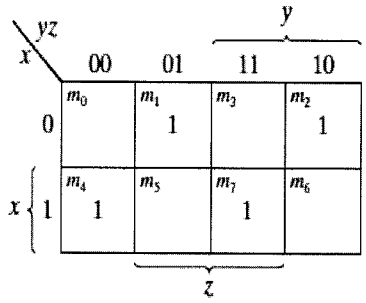
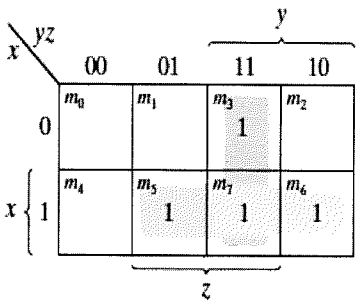
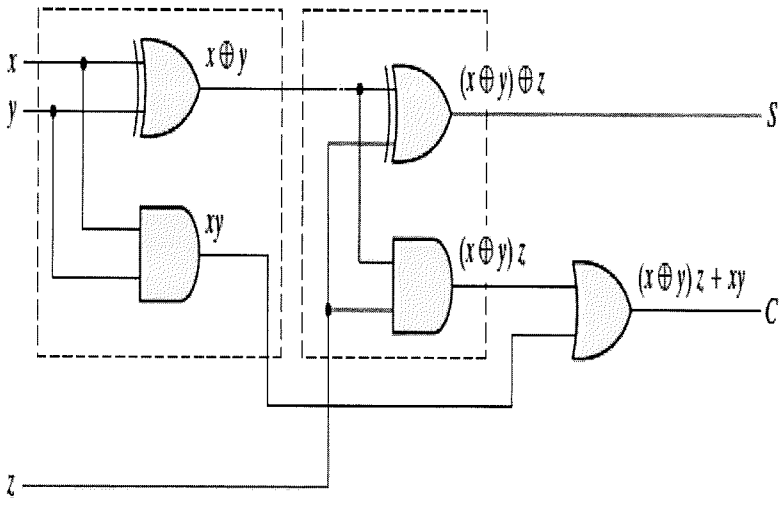
b3.b2 \ b1,b0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

For g3:

b3.b2 \ b1.b0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

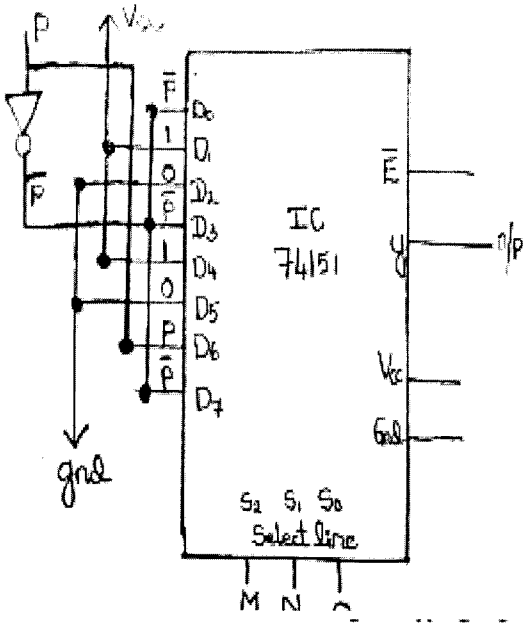
$$g_0 = b_0 b_1' + b_1 b_0' = b_0 \oplus b_1$$
$$g_1 = b_2 b_1' + b_1 b_2' = b_1 \oplus b_2$$
$$g_2 = b_2 b_3' + b_3 b_2' = b_2 \oplus b_3$$
$$g_3 = b_3$$



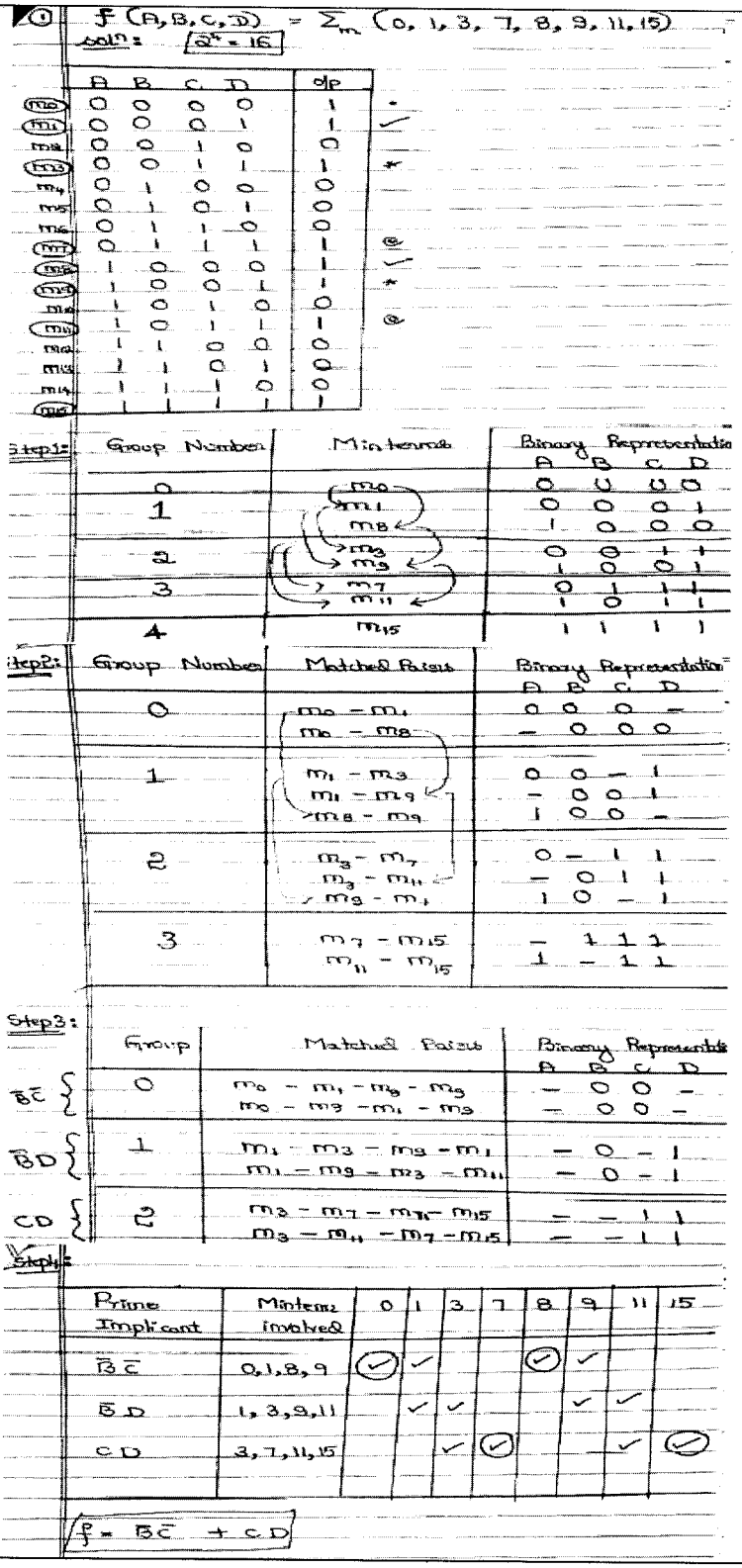
3	*Full Adder* **x y z C S** 0 0 0 0 0 0 0 1 0 1 0 1 0 0 1 0 1 1 1 0 1 0 0 0 1 1 0 1 1 0 1 1 0 1 0 1 1 1 1 1  (a) $S = x'y'z + x'yz' + xy'z' + xyz$  (b) $C = xy + xz + yz$ $S = z \oplus (x \oplus y)$ $= z'(xy' + x'y) + z(xy' + x'y)'$ $= z'(xy' + x'y) + z(xy + x'y')$ $= xy'z' + x'yz' + xyz + x'y'z$ $C = z(xy' + x'y) + xy = xy'z + x'yz + xy$ 	Truth table=2M + K-Map=2M + Logic Diagram=4M	10 min

4	$F(m,N,O,P) = \sum_m (0,2,3,\ 6,8,9,13,14)$	Truth table=4M + Logic Diagram=4M	10 min

	M	N	O	P	F	MEV	Input Connection
0	0	0	0	0	1	$\bar{P}$	D_0
1	0	0	0	1	0		
2	0	0	1	0	1	1	D_1
3	0	0	1	1	1		
4	0	1	0	0	0	0	D_2
5	0	1	0	1	0		
6	0	1	1	0	1	$\bar{P}$	D_3
7	0	1	1	1	0		
8	1	0	0	0	1	1	D_4
9	1	0	0	1	1		
10	1	0	1	0	0	0	D_5
11	1	0	1	1	0		
12	1	1	0	0	0	P	D_6
13	1	1	0	1	1		
14	1	1	1	0	1	$\bar{P}$	D_7
15	1	1	1	1	0		



Part C **(1Q x 10M = 10Marks)**

Q.No	Solution	Scheme of Marking	Max. Time required for each Question
5		Truth table=2M + Step1=2M + Step2=2M + Step3=2M + Step4=1M + Expression=1M	20 min

Q) $f(A,B,C,D) = \sum_m (0, 1, 3, 7, 8, 9, 11, 15)$

Soln: $2^4 = 16$

	A	B	C	D	o/p
m_0	0	0	0	0	1
m_1	0	0	0	1	1
m_2	0	0	1	0	0
m_3	0	0	1	1	1
m_4	0	1	0	0	0
m_5	0	1	0	1	0
m_6	0	1	1	0	0
m_7	0	1	1	1	1
m_8	1	0	0	0	1
m_9	1	0	0	1	1
m_{10}	1	0	1	0	0
m_{11}	1	0	1	1	1
m_{12}	1	1	0	0	0
m_{13}	1	1	0	1	0
m_{14}	1	1	1	0	0
m_{15}	1	1	1	1	1

Step1:

Group Number	Minterms	Binary Representation A B C D
0	m_0	0 0 0 0
1	m_1, m_8	0 0 0 1, 1 0 0 0
2	m_3, m_9	0 0 1 1, 1 0 0 1
3	m_7, m_{11}	0 1 1 1, 1 0 1 1
4	m_{15}	1 1 1 1

Step2:

Group Number	Matched Pairs	Binary Representation A B C D
0	$m_0 - m_1$	0 0 0 –
	$m_0 - m_8$	– 0 0 0
1	$m_1 - m_3$	0 0 – 1
	$m_1 - m_9$	– 0 0 1
	$m_8 - m_9$	1 0 0 –
2	$m_3 - m_7$	0 – 1 1
	$m_3 - m_{11}$	– 0 1 1
	$m_9 - m_{11}$	1 0 – 1
3	$m_7 - m_{15}$	– 1 1 1
	$m_{11} - m_{15}$	1 – 1 1

Step3:

	Group	Matched Pairs	Binary Representation A B C D
$\bar{B}\bar{C}$	0	$m_0 - m_1 - m_8 - m_9$	– 0 0 –
		$m_0 - m_8 - m_1 - m_9$	– 0 0 –
$\bar{B}D$	1	$m_1 - m_3 - m_9 - m_{11}$	– 0 – 1
		$m_1 - m_9 - m_3 - m_{11}$	– 0 – 1
CD	2	$m_3 - m_7 - m_{11} - m_{15}$	– – 1 1
		$m_3 - m_{11} - m_7 - m_{15}$	– – 1 1

Step4:

Prime Implicant	Minterms involved	0	1	3	7	8	9	11	15
$\bar{B}\bar{C}$	0,1,8,9	✓	✓			✓	✓		
$\bar{B}D$	1,3,9,11		✓	✓			✓	✓	
CD	3,7,11,15			✓	✓			✓	✓

$f = \bar{B}\bar{C} + CD$

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PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Semester: Odd Semester. 2019 - 20 | **Date**: 26 December 2019

Course Code: ECE 220 | **Time**: 1:00 PM to 4.00 PM

Course Name: DIGITAL ELECTRONICS | **Max Marks**: 80

Program & Sem: B.Tech.,(ECE&EEE) & III | **Weightage**: 40%

Instructions:

(i) Read the all questions carefully and answer accordingly.

(ii) Draw the essential diagram neatly

(iii) Bloom's Level is given for each questions, answer it accordingly.

Part A [Memory Recall Questions]

Answer all the Questions. Each Question carries 2 marks. **(10Qx2M=20M)**

1. Define De-Morgan's theorem for Boolean function: (C.O.No.1) [Knowledge]
2. Draw the logic symbol and truth table for the universal gates. (C.O.No.1) [Knowledge]
3. Implement the SOP function using NAND gate Y=A'B'+AB (C.O.No.2) [Knowledge]
4. Implement the POS function using NOR gate Y=(A'+B')(A+B) (C.O.No.2) [Knowledge]
5. Write the difference between combinational and sequential circuit. (C.O.No.3) [Knowledge]
6. Draw the full Subtractor truth table (C.O.No.3) [Knowledge]
7. Write the difference between Latch and Flip flop: (C.O.No.3) [Knowledge]
8. Draw the logic circuit for the SR latch: (C.O.No.3) [Knowledge]
9. Write the Characteristic table for JK flip flop: (C.O.No.3) [Knowledge]
10. Write the abbreviation for the following: (C.O.No.4) [Knowledge]
    a) PLA b) PLD

Part B [Thought Provoking Questions]

Answer all the Questions. Each Question carries 6 marks. (5Qx6M=30M)

11 Simplify the Boolean function using K Map $F=\sum m(0,1,4,5,6,7,8,9,12,13,14,15)$ (C.O.No.2) [Comprehension]

12 Design the Full Subtractor Combinational circuit through truth table by using two half Subtractor circuit and other basic gates. (C.O.No.3) [Comprehension]

13 Derive the truth table for full adder with inputs are A,B,Cin and outputs are Sum and Cout, and implement the same circuit by using 3 into 8 line Decoder. (C.O.No.3) [Comprehension]

14 Write the gate level modeling HDL coding for Half adder and Full Adder logic. (C.O.No.3) [Comprehension]

15 Explain the 4 bit Shift registers operation using D flip flop in the following mode.
a) SISO b) SIPO (C.O.No.3) [Comprehension]

Part C [Problem Solving Questions]

Answer both the Questions. Each Question carries 15 marks. (2Qx15M=30M)

16 Using JK flip flop, design a synchronous 4 bit counter for counting the following binary state 0000, 0001,0010.....1111. Initial state is 0000 and final state is 1111, After getting final state, the circuit should start counting over from initial state (4 bit UP counter). (C.O.No.3) [Application]

17 A sequential circuit has two JK flip flop A and B, which is described by the following flip flop input equation.

$J_A = B \quad K_A = Bx'$

$J_B = x' \quad K_B = Ax' + B'x$

Where x is the external input, A and B are the present state of flip flop.
Derive the following,
a) Logic Circuit
b) State Table
c) State Diagram
d) Next State Equations (C.O.No.3) [Application]

SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Extract of question distribution [outcome wise & level wise]

Q.NO.	C.O.NO (% age of CO)	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted] Bloom's Levels	Total Marks
			K	C	A	
PART A Q. NO 1-10	CO 01 CO 02 CO 03 CO 04	All the 5 modules	20			20
PART B Q.NO.11	CO 02	MODULE 02	-	06	-	06
PART B Q.NO.12	CO 03	MODULE 03	-	06	-	06
PART B Q.NO.13	CO 03	MODULE 03	-	06	-	06
PART B Q.NO.14	CO 03	MODULE 03	-	06	-	06
PART B Q.NO.15	CO 03	MODULE 04	-	06	-	06
PARTC Q.NO.16	CO 03	MODULE 04	-	-	15	15

PARTC Q.NO.17	CO 03	MODULE 04	-	-	15	15
	Total Marks		20	30	30	80

K =Knowledge Level C = Comprehension Level, A = Application Level

C.O WISE MARKS DISTRIBUTION:

CO 01: 4 MARKS,

CO 02: 10 MARKS,

CO 03: 64 MARKS,

CO 04: 2 MARKS

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must

be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

I hereby certify that all the questions are set as per the above guidelines.

Faculty Signature:

Reviewer Commend: CO4 covered only 2 marks. It should be balanced. Thought Provoking Questions should be asked from next Sem onwards as per the guidelines.

⇒ Faculty informed that less content was covered. (actually in syllabus also content is less).

17/12/19

Hence Approved

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SOLUTION

END TERM FINAL EXAMINATION

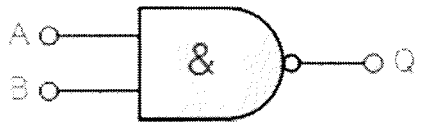
Semester: Odd Semester: 2019 - 20
Course Code: ECE220
Course Name: DIGITAL ELECTRONICS
Program & Sem: B.Tech.,(ECE) & III

Date: 26 Dec 2019
Time: 01.00pm to 04.00pm
Max Marks: 80
Weightage: 40 %

Part A [Memory Recall Questions]

1. Answer all the Questions. Each Question carries two marks. (10Qx2M= 20M)

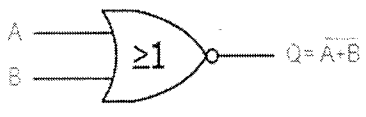
Q No	Solution	Scheme of Marking	Max. Time required for each Question
1.	Define De-Morgan's theorem for Boolean function:	[2]	2min
	$\overline{A+B} = \overline{A}.\overline{B}$ .....(1)	Equation 1 -1 M Equation 2 -1 M	
	$\overline{A.B} = \overline{A} + \overline{B}$ ... ...(2)	Equal alternate statement or logic gates also accepted	
2.	Draw the logic symbol and truth table for the universal gates.	[2]	2min



Truth Table

gate 1 -1 M
gate 2 -1 M

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

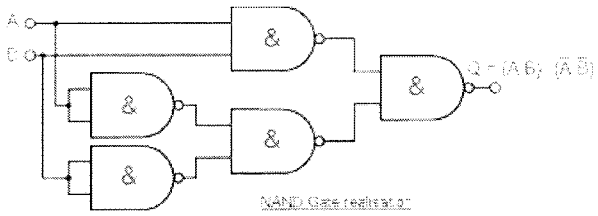


2-input NOR Gate

A	B	Q

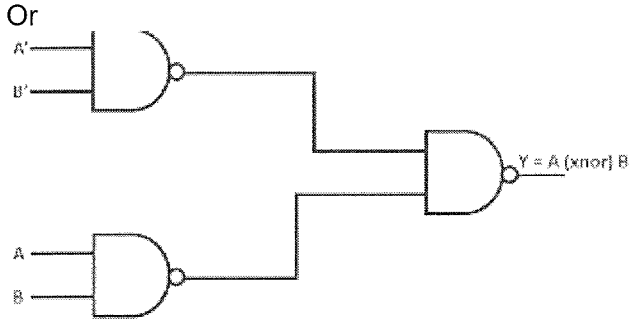
0	0	1
0	1	1
1	0	1
1	1	0

3. Implement the SOP function using NAND gate Y=A'B'+AB [2] 2min

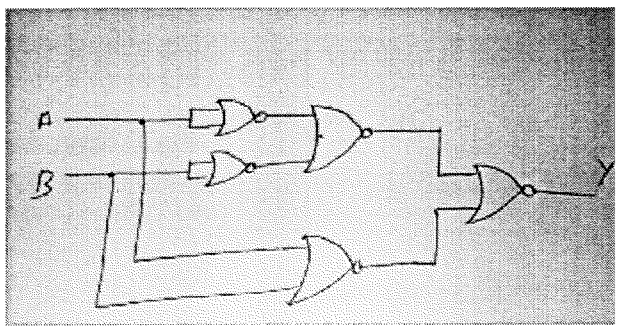


2 mark for any one diagram

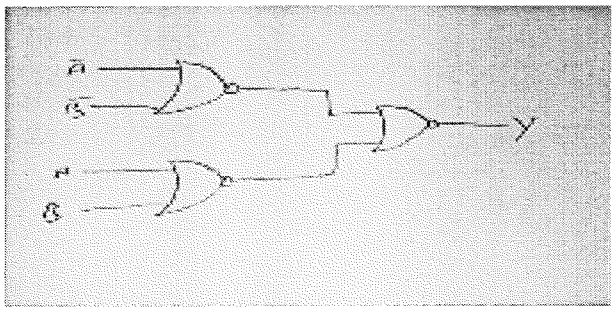
Or



4. Implement the POS function using NOR gate Y=(A'+B')(A+B) [2] 2min



2 mark for any one diagram



5. Write the difference between combinational and sequential circuit. [2] 2min

Any two difference

difference between combinational circuit and sequential circuit

combinational circuit	sequential circuit
1. The circuit whose output at any instant depends only on the input present at that instant only is known as combinationational circuit .	1. The circuit whose output at any instant depends not only on the input present but also on the past output a is known as sequental circuit
2. This type of circuit has no memory unit .	2. This type of circuit has memory unit for store past output
3. Examples of combinational circuits are half adder, full adder, magnitude comparator, multiplexer, demultiplexe r e.t.c.	3. Examples of sequential circuits are Flip flop, register, counter e.t.c.

6. Draw the full Subtractor truth table [2] 2min

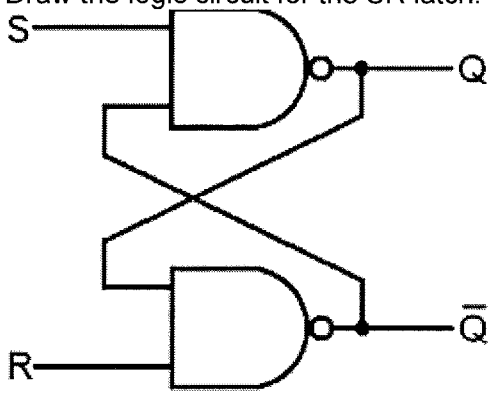
A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

7. Write the difference between Latch and Flip flop: [2] 2min

1)A latch doesn't contain any clock signal
A flip-flop contains a clock signal Any two difference

2) Level Based
Edge Based

8. Draw the logic circuit for the SR latch: [2] 2min



9. Write the Characteristic table for JK flip flop: [2] 2min

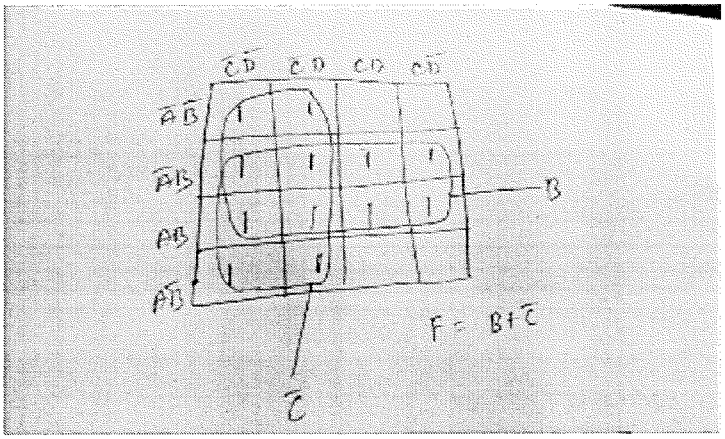
C	J	K	Q(n+1)
0	0	0	Q(n)
1	0	0	Q(n)
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q(n)}$

10. Write the abbreviation for the following: [2] 2min
    a) PLA programmable logic array
    b) PLD programmable logic devices

Part B [Thought Provoking Questions]

Answer all the Questions. Each Question carries SIX marks. (5Qx6M=30M)

11 Simplify the Boolean function using K Map F=∑m(0,1,4,5,6,7,8,9,12,13,14,15) [6] 20 min



3 mark for Kmap & Placing 1,

3 mark For grouping and Ans

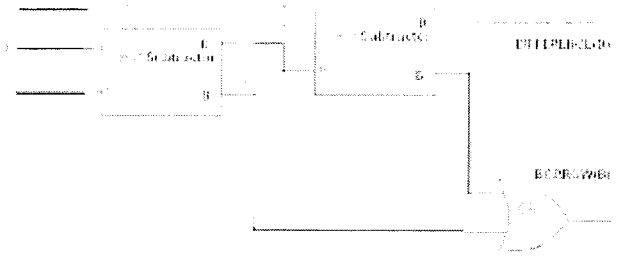
12 Design the Full Subtractor Combinational circuit through truth table by using two half Subtractor circuit and other basic gates. [6] 20 min

A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

3 mark for TT, K Map

3 mark for circuit diagram

K Map for D
K Map for Bout



13 Derive the truth table for full adder with inputs are A,B,Cin and outputs are Sum and Cout, and implement the same circuit by using 3 into 8 line Decoder. [6] 20 min

0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

3 mark for tt, Equation

3 mark for diagram

Sum=Sum of minterm of (1,2,4,7)

Cout=Sum of minterm of (3,5,6,7)

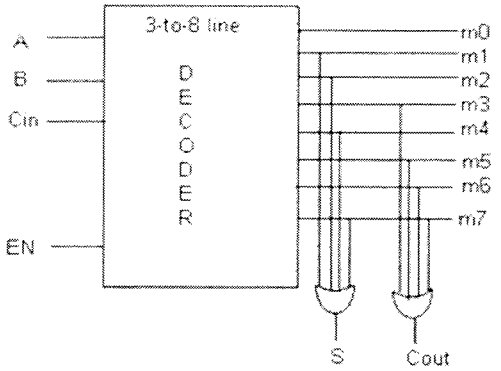


Fig1: Full Adder Implementation using 3:8 decoder

14 Write the gate level modeling HDL coding for Half adder and Full Adder logic. [6] 20 min

```
module ha(s,co,a,b);
    output s,co;
    input a,b;
    xor u1(s,a,b);
    and u2 (co,a,b);
endmodule
```

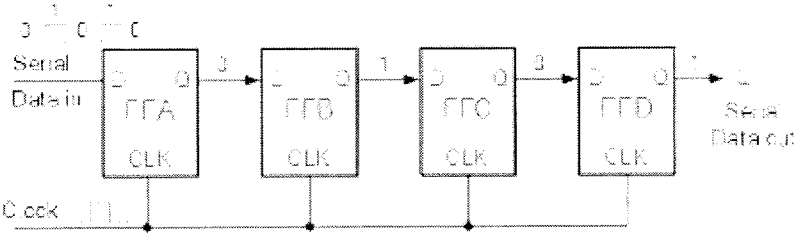
2 mark for HA

4mark for FA

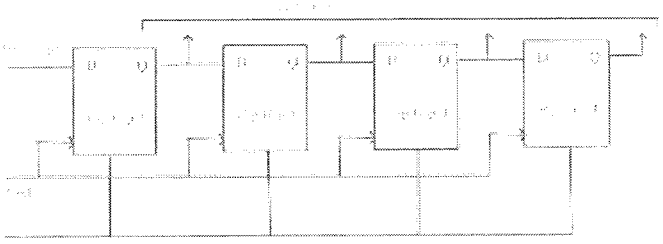
```
module fa(s,co,a,b,ci);
    output s,co;
    input a,b,ci;
    xor u1(s,a,b,ci);
    and u2(n1,a,b);
    and u3(n2,b,ci);
    and u4(n3,a,ci);
```

```
    or  u5(co,n1,n2,n3);
endmodule
```

15 Explain the 4 bit Shift registers operation using D flip flop in the following mode. [6] 20 min
a) SISO b) SIPO

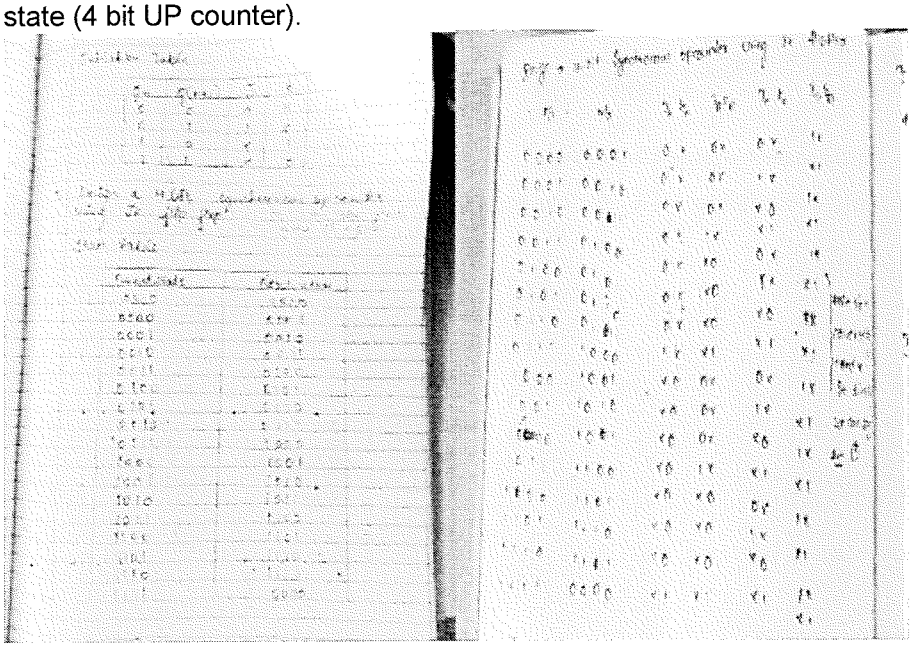


3 mark for siso block diagram, TT



3 mark for pipo block diagram, TT

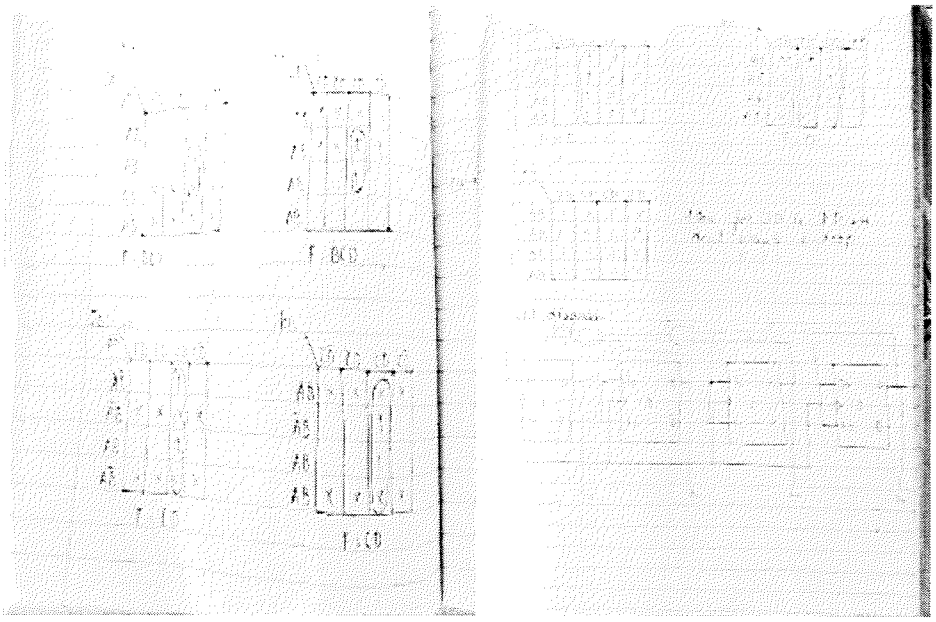
16 Using JK flip flop, design a synchronous 4 bit counter for counting the following binary state 0000, 0001,0010.....1111. Initial state is 0000 and final state is 1111, After getting final state, the circuit should start counting over from initial state (4 bit UP counter). [15] 30 min



5 marks for TT

5 marks for K map

5 Marks for circuit



17 A sequential circuit has two JK flip flop A and B, which is described by the following flip flop input equation. [15] 30 min

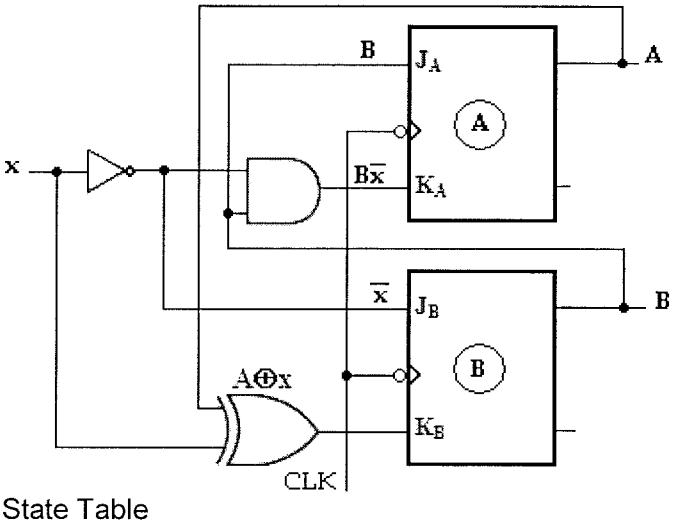
$J_A = B$ $K_A = Bx'$

$J_B = x'$ $K_B = Ax' + B'x$

Where x is the external input, A and B are the present state of flip flop. Derive the following,

a) Logic Circuit
b) State Table
c) State Diagram
d) Next State Equations

5 marks for logic circuit



3 marks for state table

2 marks for state diagram

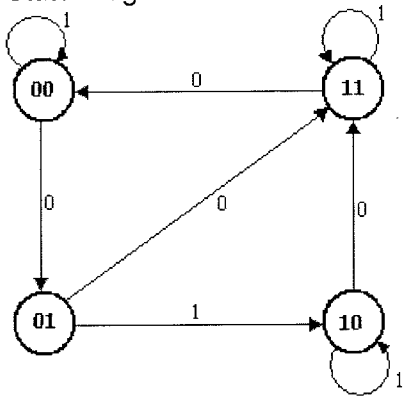
State Table

5 marks for next state diagram (either Map /other)

Present state		Inp ut	Flip-Flop Inputs				Next state	
A	B	x	$J_A = B$	$K_A = Bx'$	$J_B = x'$	$K_B = A x$	A(t+1)	B(t+1)
0	0	0	0	0	1	0	0	1

0	0	1	0	0	0	1	0	0
0	1	0	1	1	1	0	1	1
0	1	1	1	0	0	1	1	0
1	0	0	0	0	1	1	1	1
1	0	1	0	0	0	0	1	0
1	1	0	1	1	1	1	0	0
1	1	1	1	0	0	0	1	1

State Diagram



Next state equation

A(t+1)=AB'+A'B

B(t+1)=B'x'+A'x'+ABx