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 **PRESIDENCY UNIVERSITY**

  **Bengaluru**

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| **End - Term Examinations – JANUARY 2025** |
| **Date:** 09 / 01/2025 **Time:** 01:00 pm – 04:00 pm |

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| **School:** SOCSE | **Program:** B.Tech –COM/CEI/CAI/CCS/CIT/CSG/CST/ CDV/CBC/CSD/CBD/IST/ISE/ISR/ISI/ISD |
| **Course Code :**CSE2009 | **Course Name :** Computer Organization and Architecture |
| **Semester**: III | **Max Marks**:100 | **Weightage**:50% |

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| **CO - Levels** | **CO1** | **CO2** | **CO3** | **CO4** | **CO5** |
| **Marks** | **31** | **36** | **33** | **NA** | **NA** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Do not write anything on the question paper other than roll number.*

**Part A**

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| **Answer ALL the Questions. Each question carries 2marks. 10Q x 2M=20M** |
| **1** | Differentiate Memory Address Register and Memory Data Register. | 2 Marks | L1 | CO1 |
| **2** | Define clock rate. | 2 Marks | L1 | CO1 |
| **3** | Differentiate between Index Addressing Mode and Relative Addressing Mode. | 2 Marks | L1 | CO1 |
| **4** | Which is the storage, that can be accessed faster by processor.  | 2 Marks | L1 | CO2 |
| **5** | Perform -12 + 8 using 2’s complement system. | 2 Marks | L1 | CO2 |
| **6** | What is Memory mapped I/O. | 2 Marks | L1 | CO2 |
| **7** | If 32-bits are used to address a memory location, what is the maximum size of that memory. | 2 Marks | L2 | CO3 |
| **8** | Generate the control sequence for the instruction Move R1,R2 in processor with single bus organization and multiple bus organization. | 2 Marks | L1 | CO3 |
| **9** | List the four stages of pipelining used in instruction execution in a computer architecture? | 2 Marks | L1 | CO3 |
| **10** | What is WMFC? Why is this signal important. | 2 Marks | L1 | CO3 |

 **Part B**

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| **Answer the Questions Total 80 Marks.** |
| **11.** | **a.** **b.**  | Illustrate the connection between processor and memory, mention the functions of each component in the connection with proper example showing basic operating steps.Let a processor operate by a frequency 20MHtz and it executes a typical program in which 50% are register referenced instruction, 30% are memory reference instructions and 20% are branch instructions. Register referenced instruction, memory reference instructions and branch instructions take 4, 8 and 6 clock cycles respectively. then find out the total time taken by the processor to execute the program. | **10marks****10marks** | **L2****L3** | **CO1****CO1** |
| **or** |
| **12.** | **a.****b.**  | In a 16-bit machine, a Stack is stored from memory address 2500 to 1500. Initially, the stack is empty, and the stack pointer (SP) points to the address 2498. Determine the address of stack pointer, after the following operations –* Push the value ‘A’ onto the stack
* Push the value ‘B’ onto the stack
* Pop a value from the stack
* Push the value ‘C’ onto the stack
* Push the value ‘D’ onto the stack
* Pop a value from the stack

Frame the instructions to evaluate the expression E=(A+B)/(C+D) in Three address, Two address and one address instruction. | **10marks** **10marks** | **L3****L3** | **CO1****CO1** |
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| **13.** | **a.****b.** | Explain the following addressing modes – i) Absolute Mode ii) Index Mode iii) Base with Index Mode iv)Auto-increment Mode v) Relative Mode.Perform the division of 14÷3 using the Integer Restoring division method | **10 Marks****10 Marks** | **L2****L2** | **CO2****CO2** |
| **or** |
| **14.** | **a.****b.** | What is the main limitation of a Ripple Carry Adder. Illustrate using expressions of G and P how the Carry Lookahead Adder overcomes the limitation. Describe Booth's algorithm for signed-operand multiplication and solve −12× -10. | **10 Marks****10 Marks** | **L2****L3** | **CO2****CO2** |

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| **15.** | **a.****b.** | Design a DMA interface and explain its working with a suitable diagramRegister R1 and R2 of computer holds the value 3200 and 4600 respectively. Find the effective address of the source operand in each of the following instructions? (Assume 64-bit word length and each are individual instructions)1. Load 20(R1), R2
2. Subtract (R1) +, R5
3. Add – (R2), R5
4. Store  30(R1,R2), (R5)
5. Move  R1, R5
 | **10Marks****10Marks** | **L2****L3** | **CO1****CO1** |
| **Or** |
| **16.** | **a.****b.** |  Explain interrupt-driven I/O communication and the role of ISR to solve the interrupts.Suppose the main memory consists of 512 blocks of 8 words each and cache consists of 64 blocks. How many bits are required for the main memory address? How many bits are there in each of Tag, block/set and word fields for Direct, Associative, and Set- Associative mapping techniques? (Note: There are 4 cache blocks in each set). | **10 Marks****10 Marks** | **L2****L3** | **CO3****CO3** |

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| **17.** | **a.****b.** | Illustrate single-bus organization with a neat diagram. Generate and explain the control sequence for execution of complete instruction [Add R4,R5] in single- bus organization.Illustrate the concept of pipelining and explain the different types of hazards in pipelining. | **10 Marks****10 Marks** | **L2****L2** | **CO3****CO3** |
| **Or** |
| **18.** | **a.****b.** | Illustrate multiple-bus organization with a neat diagram. Generate and explain the control sequence for execution of complete instruction [Add R4,R5] in multiple- bus organization.How is the performance increased by using pipelining concept? What are the possible hazards in pipelining. Explain. | **10 Marks****10 Marks** | **L2****L2** | **CO3****CO3** |