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**PRESIDENCY UNIVERSITY**

**Bengaluru**

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| **End - Term Examinations – JANUARY 2025** |
| Date: 07 – 01- 2025 Time: 09:30 am – 12:30 pm |

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| **School:** SOE | **Program:** B. Tech-ECE | |
| **Course Code :** ECE3046 | **Course Name :** Low Power VLSI Design | |
| **Semester**: VII | **Max Marks**:100 | **Weightage**: 50% |

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| **CO - Levels** | **CO1** | **CO2** | **CO3** | **CO4** | **CO5** |
| **Marks** | **12** | **16** | **36** | **36** |  |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Do not write anything on the question paper other than roll number.*

**Part A**

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| **Answer ALL the Questions. Each question carries 2marks. 10Q x 2M=20M** | | | | |
| **1** | What is need for low power VLSI design? | **2 Marks** | **L1** | **CO1** |
| **2** | How can the short circuit current be reduced in a CMOS circuit? | **2 Marks** | **L1** | **CO1** |
| **3** | What is activity in Event-driven logic simulation? | **2 Marks** | **L1** | **CO2** |
| **4** | Define GLS. | **2 Marks** | **L1** | **CO2** |
| **5** | Why is transistor and gate sizing required? | **2 Marks** | **L1** | **CO3** |
| **6** | Define precomputation Logic. | **2 Marks** | **L1** | **CO3** |
| **7** | What is signal gating? | **2 Marks** | **L1** | **CO3** |
| **8** | Illustrate state machine encoding. | **2 Marks** | **L1** | **CO4** |
| **9** | What is the difference between NAP and SLEEP mode? | **2 Marks** | **L1** | **CO4** |
| **10** | Define zero skew. | **2 Marks** | **L1** | **CO4** |

**Part B**

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| **Answer the Questions Total 80 Marks.** | | | | | |
| **11.** | **a.** | The leakage power dissipation is one of the main sources of power dissipation. It is a major concern for portable devices, as it can increase power consumption and reduce battery life.  (i)Describe reverse diode leakage current.(8)  (ii) Write short note on internal switching energy of a 4 transistor NAND gate.(12) | **20 Marks** | **L2** | **CO1&2** |
| **Or** | | | | | |
| **12.** | **a.** | **(i**) DIBL is the main short-channel effect of short-channel devices. Describe DIBL  (ii) The designer can apply low-power techniques at the architecture level. Explain the pipelining architecture and its impact on power reduction. | **20 Marks** | **L2** | **CO1&2** |
|  |  |  |  |  |  |
| **13.** | **a.** | (i) The low-power technique is also implemented at the circuit level. Describe network restructuring and reorganization.  (i) Realize the Boolean function f=((D+E+A). (B+C))’. Find an equivalent CMOS inverter circuit for simultaneous switching of all input. Given (W/L)P=15 for all PMOS and (W/L)N=10 for all NMOS. | **20 Marks** | **L3** | **CO3** |
| **Or** | | | | | |
| **14.** | **a.** | The logical encoding has a great impact on switching activity of CMOS circuit. Illustrate logical encoding and prove that gray code is an efficient coding than binary coding for low power counter circuit design. | **20 Marks** | **L3** | **CO3** |

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| **15.** | **a.** | (i) Performance management is an important issue in architecture-level management. Explain power and performance management.  (ii) The control data flow graph is starting to derive DSP hardware implementation. Draw the control data flow graph for the equation Yn= anbn+3an-1. | **20 Marks** | **L3** | **CO4** |
| **Or** | | | | | |
| **16.** | **a.** | The full-swing clock increases the power dissipation of the circuit. Hence, the reduced swing clock circuit is designed to reduce power dissipation.  (i)Describe the simplified form of reduced swing clock circuit.  (ii) Write short note on operator reduction with suitable example. | **20 Marks** | **L3** | **CO4** |

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| **17.** | **a.** | The FF is the first and last element of the signal delay path and consumes more power.  (i)Explain special FF for low power applications.  (ii) Describe Gate reorganization. | **20 Marks** | **L3** | **CO3&4** |
| **Or** | | | | | |
| **18.** | **a.** | The adaptive design is an effective method of reducing power dissipation of the circuit.  (i)Explain adaptive performance management by voltage control.  (ii) Write a short note on the need for buffer in clock tree. | **20 Marks** | **L3** | **CO3&4** |

**\*\*\*\*\* BEST WISHES \*\*\*\*\***