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 **PRESIDENCY UNIVERSITY**

  **Bengaluru**

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| **End - Term Examinations – JANUARY 2025** |
| Date: 07-01-2025 Time: 09:30 am – 12:30 pm |

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| **School:** SOE | **Program:** B.Tech-ECE |
| **Course Code:** ECE3050 | **Course Name:** Design for Testability |
| **Semester**: VII | **Max Marks**:100 | **Weightage**:50% |

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| **CO - Levels** | **CO1** | **CO2** | **CO3** | **CO4** |
| **Marks** | **22** | **24** | **26** | **28** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Do not write anything on the question paper other than roll number.*

**Part A**

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| **Answer ALL the Questions. Each question carries 2marks. 10Q x 2M=20M** |
| **1** | What are the properties of a testable circuit? | **2 Marks** | **L1** | **CO4** |
| **2** | Define and generate singular cover for AND gate | **2 Marks** | **L1** | **CO1** |
| **3** | What is role of DFT Engineer? | **2 Marks** | **L1** | **CO3** |
| **4** | Name two test vector generation techniques for detecting only single faults but not multiple faults? | **2 Marks** | **L1** | **CO2** |
| **5** | To quantify of the ease of testing two terms are commonly used in DFT i.e controllable and Observable. Define what is controllability and Observability? | **2 Marks** | **L1** | **CO2** |
| **6** | What are the different types of fault classes? | **2 Marks** | **L1** | **CO4** |
| **7** | Define primitive polynomial with an example. | **2 Marks** | **L1** | **CO4** |
| **8** | Define and generate singular cover for EX-OR gate | **2 Marks** | **L1** | **CO1** |
| **9** | How many single stuck-at faults are present in the below combinational circuit? | **2 Marks** | **L1** | **CO3** |
| **10** | What is ATE? What it does? | **2 Marks** | **L1** | **CO4** |

**Part B**

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| **Answer the Questions Total 80 Marks.** |
| **11.** | **a.** | Generate the test vector for finding SA0 fault on line x1 of the following figure using Boolean difference method with all simplification steps to be mentioned? | **20 Marks** | **L3** | **CO1** |
| **Or** |
| **12.** | **a.** | **i**) a. Find the test vector to be generated to detect faults at the input(A.B) and output(F) pf the OR gate which are stuck at 0 and 1 in the given circuit.ii)Design truth tables for the fault-free circuit and the faulty circuits for all possible single stuck-at faults.iii) Elaborate on typical defects in VLSI chips with examples.iv) Find the test vector to be generated to detect stuck at 0 faults at net ‘d’ in the given circuit | **5+5+5+5****Marks** | **L2** | **CO1** |
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| **13.** | **a.** | i) Scan cell design is the most widely used structured DFT methodology. Explain about Edge triggered Muxed D Scan Cell design and test operation with suitable diagrams and waveforms?ii) In VLSI engineering a common fault after stuck at fault model is a bridging fault. Discuss the different types of bridging faults with an example. | **(10+10) Marks** | **L2** | **CO2** |
| **Or** |
| **14.** | **a.** | i) How the path sensitization method is used to generate a test pattern for combinational circuits? Find the test vector using path sensitization method for the given figure.ii) Find the test vector for the given figure using truth table for faulty and fault free circuit | **(10+10)Marks** | **L3** | **CO2** |

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| **15.** | **a.** | i) An automated test pattern generator called Built-in Self-Test(BIST) is utilized to find faults. Discuss the BIST logic system architecture?ii) What is the advantage of pseudo exhaustive pattern generator over exhaustive pattern generator?iii) Write a note on ad hoc DFT methods.iv) Explain why BIST is the preferred form of DFT? | **5+5+5+5 Marks** | **L2** | **CO3** |
| **Or** |
| **16.** | **a.** | i) Scan Compression is a DFT technique that reduces the testing time. Discuss the importance of scan compression technique with neat block diagram.ii) Discuss the economic case for BIST using some chip level testability problems. | **(10+10) Marks** | **L2** | **CO3** |

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| **17.** | **a.** | i) Write a detail description about LFSR types and properties with a neat sketch? Generate the test sequence using given characteristic polynomial X5 +X3+X+1?ii) Write about signature analysis / Transition count response compaction with a neat sketch for given circuit faulty and fault free circuit where a=10101 b=10100 c=11100 d=10100 considering SA0 fault on line b. | **(10+10)Marks** | **L3** | **CO4** |
| **Or** |
| **18.** | **a.** | i) Explain the steps in D algorithm? Generate the test vector for SA1 fault on the line h as shown in figure using D- algorithm? | **20****Marks** | **L3** | **CO4** |

**\*\*\*\*\* BEST WISHES \*\*\*\*\***