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**PRESIDENCY UNIVERSITY**

**Bengaluru**

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| **End - Term Examinations – JANUARY 2025** |
| **Date:** 13 – 01- 2025 **Time:** 09:30 am – 12:30 pm |

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| **School:** SOE | **Program:** B. Tech ECE | |
| **Course Code :** ECE3090 | **Course Name :** Digital System Design using VERILOG | |
| **Semester**: V | **Max Marks**: 100 | **Weightage**: 50% |

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| **CO - Levels** | **CO1** | **CO2** | **CO3** | **CO4** | **CO5** |
| **Marks** | **18** | **24** | **43** | **50** | **------** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Do not write anything on the question paper other than roll number.*

**Part A**

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| **Answer ALL the Questions. Each question carries 2marks. 10Q x 2M=20M** | | | | |
| **1** | In Verilog, data type help in defining how data is stored, transmitted, and manipulated within a digital design. How many data types are available in Verilog and what do they describe? | **2 Marks** | **L** | **CO1** |
| **2** | In Verilog, a design can be modeled in three different styles (data flow, structural or gate level and behavioral) or in a mixed style. List at least two characteristics of data flow modeling. | **2 Marks** | **L** | **CO1** |
| **3** | Verilog uses left shift and right shift operations. If X = 4'b0110, then  What will be the value of Y after the expression Y = X << 1; is executed? | **2 Marks** | **L** | **CO1** |
| **4** | In Verilog, operators are used to perform various operations on data. What will be the value of Y after the expression Y = {A, B[0], C[1], D[2]} is executed? The values of A, B, C and D are:  A = 1'b1, B = 2'b00, C = 2'b10, D = 3'b110 | **2 Marks** | **L** | **CO1** |
| **5** | Draw the circuit for the following keyword of Verilog “buffif0” and “notif0”. | **2 Marks** | **L** | **CO2** |
| **6** | A cmos device can be modeled with an nmos and a pmos device. Draw the symbol for a cmos device with its proper labels. | **2 Marks** | **L** | **CO2** |
| **7** | In Verilog, a design can be modeled in three different styles (data flow, structural or gate level and behavioral) or in a mixed style. Differentiate between data flow and behavioral models on the basis of the types of statements they use. | **2 Marks** | **L** | **CO3** |
| **8** | Verilog has two types of procedural assignment - Blocking and Non-blocking. Differentiate between them using an example. | **2 Marks** | **L** | **CO3** |
| **9** | Behavioral modeling represents digital circuits at a functional and algorithmic level. List the two important keyword used in behavioral modeling. | **2 Marks** | **L** | **CO3** |
| **10** | A repeat loop is used to execute statements a given number of times. Write a repeat loop statement which repeats the clock 7 times to enable a signal en = 1. | **2 Marks** | **L** | **CO3** |

**Part B**

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| **Answer the Questions Total 80 Marks** | | | | | |
| **11.** | **a.** | A multiplexer is a combinational circuit which receives data using ‘2^n’ input lines and routes them to only one output line, using ‘n’ select input lines. You need to design a 4-to-1 multiplexer, whose truth table is given below. Do the following:  (a) Write the **Data Flow Model** Verilog code for a main module which implements the above 4-to-1 multiplexer, using conditional operators.  (b) Write the Verilog test bench which instantiates the above main module.   |  |  |  | | --- | --- | --- | | **s0** | **s1** | **out** | | 0 | 0 | d0 | | 0 | 1 | d1 | | 1 | 0 | d2 | | 1 | 1 | d3 | | **10**  **Marks** | **L** | **CO1** |
| **or** | | | | | |
| **12.** | **a.** | A decoder is a combinational circuit which has ‘n’ input lines and ‘2^n’ output lines with an enable input. Consider the following circuit shown in the figure below, which is a 3:8 decoder. Assume that a 2:4 decoder module is already available for instantiation (named DEC\_2\_4), do the following:  (a) Write the **Structural (Gate Level) Model** Verilog code for a main module which implements the above 3:8 decoder.  (b) Write the Verilog test bench which instantiates the above main module. | **10**  **Marks** | **L** | **CO2** |
|  |  |  |  |  |  |
| **13.** | **a.** | Switch level modeling in Verilog is a method used to describe digital circuits by focusing on the behavior of MOS transistors as electronic switches. For the circuit shown below, do the following:  (a) Write the switch level Verilog code as the main module.  (b) Write the Verilog test bench which instantiates the above main module.  **Note:** Make sure that the internal and external signals are properly labeled.CMOS Logic Gates Explained - ALL ABOUT ELECTRONICS | **10**  **Marks** | **L** | **CO2** |
| **or** | | | | | |
| **14.** | **a.** | The truth table of a typical digital circuit has been given below. The output ‘Y’ in binary indicates the number of ‘1s’ present in the input B. Do the following:  (a) Write the Verilog code for a main module which implements the circuit as in truth table using ***if – else*** statement.  (b) Write the Verilog test bench which instantiates the above main module.   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **B2** | **B1** | **B0** | **Y1** | **Y0** | | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 1 | 0 | 1 | | 0 | 1 | 0 | 0 | 1 | | 0 | 1 | 1 | 1 | 0 | | **10**  **Marks** | **L** | **CO3** |

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| **15.** | **a.** | The truth table of a typical digital circuit has been given below. The output ‘Y’ in binary indicates the number of ‘1s’ present in the input B. Do the following:  (a) Write the Verilog code for a main module which implements the circuit as in truth table using ***case*** statement.  (b) Write the Verilog test bench which instantiates the above main module.   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **B2** | **B1** | **B0** | **Y1** | **Y0** | | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 1 | 0 | 1 | | 0 | 1 | 0 | 0 | 1 | | 0 | 1 | 1 | 1 | 0 | | **10**  **Marks** | **L** | **CO3** |
| **Or** | | | | | |
| **16.** | **a.** | A Combinational UDP take the inputs and produce the output value by looking up the corresponding entry in the state table. You need to design a combinational UDP which implements a 2:1 multiplexer. Do the following:  (a) Write the Verilog code for a main module which implements the above 2:1 multiplexer using combinational UDP.  (b) Write the Verilog test bench which instantiates the above main module. | **10**  **Marks** | **L** | **CO4** |

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| **17.** | **a.** | A shift register shifts a bit in subsequent stages based on applied clock using various configurations (like SISO, SIPO, PISO and PIPO). You need to design a shift register which operates like in the following manner – at negative edge of clock, if reset is low output will be set to 0, if reset is high it loads a new value to output (i.e. if load\_en=1), if reset is high and load\_en =0 then it shifts the bits to left from LSB side to MSB side by inserting a 0 at LSB. Do the following:  (a) Write the Verilog code for a main module which implements the above shift register using ***for loop*** and which shifts 4 bits.  (b) Write the Verilog test bench which instantiates the above main module. | **15**  **Marks** | **L** | **CO3** |
| **Or** | | | | | |
| **18.** | **a.** | A shift register shifts a bit in subsequent stages based on applied clock using various configurations (like SISO, SIPO, PISO and PIPO). You need to design a shift register which operates like in the following manner – at negative edge of clock, if reset is low output will be set to 0, if reset is high it loads a new value to output (i.e. if load\_en=1), if reset is high and load\_en =0 then it shifts the bits to left from LSB side to MSB side by inserting a 0 at LSB. Do the following:  (a) Write the Verilog code for a main module which implements the above shift register using ***while loop*** and which shifts 4 bits.  (b) Write the Verilog test bench which instantiates the above main module. | **15**  **Marks** | **L** | **CO3** |

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| **19.** | **a.** | A task is like a procedure; it provides the ability to execute common pieces of code from several different places in a description. Tasks are declared with the keywords ***task*** and ***endtask***. You need to detect the number of zeros (0s) in an 8-bit number. Do the following:  (a) Write the Verilog code for a main module which has a task ‘zeroscounter’.  (b) Write the Verilog test bench which instantiates the above main module. | **15**  **Marks** | **L** | **CO3** |
| **Or** | | | | | |
| **20.** | **a.** | A function is like a procedure; it provides the ability to execute common pieces of code from several different places in a description. Functions are declared with the keywords ***function*** and ***endfunction.*** You need to write two functions for the following Gray Code to Binary converter shown in figure below. Do the following:  (a) Write the Verilog code for a main module which has two functions namely ‘**buf\_func**’ and ‘**xor\_func**’, in order to model the above converter.  (b) Write the Verilog test bench which instantiates the above main module. | **15**  **Marks** | **L** | **CO3** |

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| **21.** | **a.** | A sequence detector detects a sequence and designed using state diagram and by forming the state table. For a 4-bit Sequence detector which detects a sequence “**1011**” and uses **MOORE** Model by considering **Overlapping** case, do the following:  (a) Draw the state diagram.  (b) Write the Verilog code of its main module  (c) Write the Verilog test bench which instantiates the above main module. | **20**  **Marks** | **L** | **CO4** |
| **Or** | | | | | |
| **22.** | **a.** | A sequence detector detects a sequence and designed using state diagram and by forming the state table. For a 4-bit Sequence detector which detects a sequence “**1011**” and uses **MOORE** Model by considering **Non-overlapping** case, do the following:  (a) Draw the state diagram.  (b) Write the Verilog code of its main module  (c) Write the Verilog test bench which instantiates the above main module. | **20**  **Marks** | **L** | **CO4** |

**\*\*\*\*\* BEST WISHES \*\*\*\*\***