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**PRESIDENCY UNIVERSITY**

**Bengaluru**

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| **End - Term Examinations – JANUARY 2025** |
| **Date:** 09 / 01/2025 **Time:** 01:00 pm – 04:00 pm |

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| **School:** SOE | **Program :** B.Tech (ECE) | |
| **Course Code :** ECE2002 | **Course Name :** DIGITAL ELECTRONICS | |
| **Semester** : III | **Max Marks** : 100 | **Weightage** : 50% |

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| **CO - Levels** | **CO1** | **CO2** | **CO3** | **CO4** | **CO5** |
| **Marks** | **15** | **15** | **35** | **35** | **NA** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Do not write anything on the question paper other than roll number.*

**Part A**

|  |  |  |  |  |  |
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| **Answer ALL the Questions. Each question carries 2marks. 10Q x 2M=20M** | | | | | |
| **1** | A \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ logic circuits depends only on the present inputs, not on previous output. And it does not have memory and no feedback element. | **2 Marks** | **L1** | | **CO3** |
| **2** | Write Boolean Sum output equation of Half Adder in PoS form : | **2 Marks** | **L1** | | **CO3** |
| **3** | In N into 2^N line decoder, the binary information are decoded into…………….. | **2 Marks** | **L1** | | **CO3** |
| **4** | Write the name of the logic circuit which accepts several input data and allows only one of them at a time to the output with the help of selection lines: | **2 Marks** | **L1** | | **CO3** |
| **5** | Identify a logic gate and write the truth table which is used to compare the equality of two one bit binary number: | **2 Marks** | **L1** | | **CO3** |
| **6** | Identify the flip-flop which has forbidden input case and for which input combination, the forbidden case was happened? | 2 Marks | | **L1** | **CO4** |
| **7** | For designing a **‘4’** bit Synchronous Counter, Determine How many number of D flip-flops are needed? | 2 Marks | | **L1** | **CO4** |
| **8** | In a JK flip-flop, which input combination causes the toggle output of its current state? | 2 Marks | | **L1** | **CO4** |
| **9** | Write the Characteristics table of S R flipflop: | 2 Marks | | **L1** | **CO4** |
| **10** | Write the Characteristics Equation of S R Flip Flop: | 2 Marks | | **L1** | **CO4** |

**Part B**

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| **Answer the Questions. Total Marks 80** | | | | | |
| **11.** | **a.**  **b.** | A student provided with D Flip flop for his lab exercise. But he need J K Flipflop for his experiment. By using characteristic and Excitation table help the student to convert D to JK flip flop:  Using JK flipflop, Design a 3 bit Synchronous UP Counter which is used to count the clock from 0 to 7: | **10 Marks**  **15 Marks** | **L3** | **CO4** |
| **Or** | | | | | |
| **12.** | **a.** | A sequential circuit has two JK flip-flops A and B, two input x & y. and one output ‘z’. The flipflop input equations and circuit output equation are  JA= B’y’+BxKA=B’xy’ JB=A’x KB=A+xy’ z=(A+B)x’y’ | **25 Marks** | **L3** | **CO4** |
|  |  |  |  |  |  |
| **13.** | **a.**  **b** | Using 8x1 MUX, design the given Boolean function Y:  Y=Σ( 1,3,4,5,11,12, 13,14,15)  Derive the truth table of Full Adder and design the same circuit by using minimum number of 2-input ExOR gate, AND gate and OR gate | **10 Marks**  **15 Marks** | **L3** | **CO3** |
| **Or** | | | | | |
| **14.** | **a.**  **b.** | Design Full Subtractor using 3 into 8-line Decoder:  Design a combinational circuit, Which is used for Priority based 4 into 2 line Data Encoder: | **10 Marks**  **15 Marks** | **L3** | **CO3** |

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| **15.** | **a.** | A student is provided with minimum Number of NAND gates and a 4Variale Boolean function (W’+ Y’)( X+ Z)( W’+ X).  For designing the Boolean function into digital circuits, he has to do the following. Help the student to design circuit:  i) Convert into Canonical PoS.  ii)Simplify the function in SoP form using K map.  iii)Draw the logic circuit. | **15**  **Marks** | **L2** | **CO2** |
| **Or** | | | | | |
| **16.** | **a.** | For the given Boolean function,  Y=Σ(0,1,4,5,6,7, 13,14)+DCΣ(11, 15), Derive the following:  i) Canonical PoS.  ii)Simplify the function in PoS form using K map.  iii)Draw the logic circuit. | **15 Marks** | **L2** | **CO2** |

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| **17.** | **a.** | Derive the following:   1. OR gate output using minimum NAND gate: 2. ExOR gate truth table and logic circuit using   minimum NAND gate:   1. ExNOR gate truth table and logic circuit using   minimum NOR gate: | **15**  **Marks** | **L2** | **CO1** |
| **Or** | | | | | |
| **18.** | **a.** | Find the following:  i)Decimal value of given Binary (101010.1001)2 is \_\_\_\_\_\_\_\_\_  ii)Octal value of (101111.1011)2 is \_\_\_\_\_\_\_\_\_\_\_\_  iii)Hexa value of (10010110011.100101)2 is \_\_\_\_\_\_\_\_\_\_  iv)Draw the OR gate output using minimum NAND gate:  v)The octal equivalent of hexadecimal ( BAC ) is \_\_\_\_\_\_\_ | **15**  **Marks** | **L2** | **CO1** |