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**PRESIDENCY UNIVERSITY**

**Bengaluru**

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| **End - Term Examinations –JANUARY 2025** |
| **Date:** 09/01/2025 **Time:** 01:00 pm – 04:00 pm |

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| **School:** SOE | **Program**: ECE(VLSI) | |
| **Course Code :** ECE2013 | **Course Name :** Digital System Design Using HDL | |
| **Semester**: III | **Max Marks**:100 | **Weightage**: 50% |

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| **CO - Levels** | **CO1** | **CO2** | **CO3** | **CO4** | **CO5** |
| **Marks** | **28** | **24** | **26** | **22** | **--** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Do not write anything on the question paper other than roll number.*

**Part A**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Answer ALL the Questions. Each question carries 2marks. 10Q x 2M=20M** | | | | |
| **1** | Which are the famous HDL languages? | **2 Marks** | **R** | **CO1** |
| **2** | What are the value sets Verilog supports | **2 Marks** | **R** | **CO1** |
| **3** | Explain the different datatypes of Verilog . | **2 Marks** | **R** | **CO1** |
| **4** | Give two example for compiler directives in Verilog | **2 Marks** | **R** | **CO1** |
| **5** | What is the output for expressions given A= 3’b110, b = 1’b1, c=4’b1101  Y = 2{a[1], b, c[2]} | **2 Marks** | **U** | **CO2** |
| **6** | Explain the components in module | **2 Marks** | **R** | **CO2** |
| **7** | What is the difference between ROM and PLA | **2 Marks** | **R** | **CO4** |
| **8** | Differentiate between Mealy and Moore FSM | **2 Marks** | **R** | **CO3** |
| **9** | What are the different hazard types in combinational networks | **2 Marks** | **R** | **CO3** |
| **10** | Explain 1 bit overlap and non overlap in sequence detector with example | **2 Marks** | **U** | **CO3** |

**Part B**

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| **Answer the Questions Total 80 Marks.** | | | | | |
| **11.** | **a.**  **b.** | With the help of flow chart explain the typical VLSI design flow  Explain the various IC design methodologies | **20 Marks** | **R** | **CO1** |
| **Or** | | | | | |
| **12.** | **a.**  **b.** | Write a Verilog code to implement SR Flip Flop, D Flip Flop using behavioral style  Explain the following operators in Verilog   * + - 1. Shift operators       2. Relational operators | **20 Marks** | **U** | **CO1** |
|  |  |  |  |  |  |
| **13.** | **a.** | Implement a full Subtractor circuit using gate level, data flow and behavioral styles. Write any one test bench code to verify the output additionally draw the expected output waveforms according to the test bench code | **20 Marks** | **U** | **CO2** |
| **Or** | | | | | |
| **14.** | **a.**  **b.** | Develop a sequence detector to detect a sequence 1010 with no overlap using Mealy and Moore style.  Write the Verilog design code and the test bench code for the above sequence detector (for any one) | **20 Marks** | **A** | **CO2** |

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| **15.** | **a.**  **b.** | Build a combinational logic circuit using an ROM. The Combinational logic circuit will take a 3 bit number and calculate its square. Choose the ROM of suitable size. Identify the number of input and outputs in your design. How many words can be stored in the ROM memory and what is the size of each word?  Build a the full adder circuit using a PAL | **20 Marks** | **A** | **CO4** |
| **Or** | | | | | |
| **16.** | **a.** | With a neat figure explain the working of parallel multiplier? Multiply two numbers 13 \* 11. Show all steps for multiplication | **20 Marks** | **A** | **CO4** |

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| **17.** | **a.**  **b.** | Integrated circuit (IC) design and development is the process of creating electronic circuits on silicon chips for a variety of devices. Explain this process by using Y chart  Explain structural, behavioral and physical hierarchy in the IC design process | **20 Marks** | **R** | **CO3** |
| **Or** | | | | | |
| **18.** | **a.**  **b.** | What are the different types of semi-custom ICs  How are full custom IC different from semi-custom ICs | **20 Marks** | **R** | **CO3** |

**\*\*\*\*\* BEST WISHES \*\*\*\*\***