Roll No.												

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

TEST 1

Sem & AY: Odd Sem 2019-20
Course Code: EEE 316
Course Name: POWER SEMICONDUCTOR DEVICES
Program & Sem: B.Tech (EEE) & V DE

Date: 30.09.2019
Time: 2.30 PM to 3.30 PM
Max Marks: 40
Weightage: 20%

Instructions:

i. Read the question properly and answer accordingly.
ii. Question paper consists of 3 parts.
iii. Scientific and Non-programmable calculators are permitted.

Part A [Memory Recall Questions]

Answer all the Questions. Each Question carries ten marks. (10Qx1M=10M)
(Q.i-x)(C.O.NO.1) [Knowledge]

1.

i. The reverse current in a diode is of the order of ....

A.kA
B.mA
C.μA
D.A

ii. If the doping level in a crystal diode is increased, the width of depletion layer...

A.remains the same
B.is decreased
C.in increased
D.none of the above

iii. When PN junction is in forward bias, by increasing the battery voltage

A.Circuit resistance increases
B.Current through P-N junction increases
C.Current through P-N junction decreases
D.None of the above happens

iv . As a PN junction is forward biased

A.Holes as well as electrons tend to drift away from the junction
B.The depletion region decreases
C. The barrier tends to breakdown
D.None of the above

v. For a PN junction, the junction current will be zero when

A.The two junctions are short circuited
B.Holes and electrons get neutralized by equal numbers
C.The number of minority carriers crossing the junction equals the number of majority carriers
D.Either minority carriers or majority carriers disappear

vi. Which of the following is true for the active region of an npn transistor?
A.The collector current is directly proportional to the base current
B.The potential difference between the emitter and the collector is less than 0.4 V
C.All of the mentioned
D.None of the mentioned

vii. Collector region of BJT is always

A.lightly doped
B.moderately doped
C.heavily doped
D.not doped

viii. If collector current is 2mA and base current is 0.5mA than emitter current will be

A.10mA
B.2.5mA
C.1.5mA
D.4mA

ix. Under which condition, collector emitter voltage 'V_{CE}' is equals to supply collector voltage 'V_{CC}'?

A.cutoff region
B.linear region
C.saturation region
D.breakdown region

x. When collector emitter voltage reaches sufficiently high, reverse biased base-collector goes to

A.increase
B.decrease
C.breakdown
D.forward biased

Part B (Thought Provoking Questions)

Answer all the Questions. (3Q=20M)

2. The holes and electrons concentration, decides the layer type of semiconductor devices. What is meant by P^{+}-N^{-} junction? Discuss the formation of depletion layer in p-n junction of power diode? [8 M]

   (C.O.NO.1) [Comprehension]

3. What is the difference between beta and forced beta for BJT's? – [2 M]

   (C.O.NO.1) [Knowledge]

4. Any ideal switching device behaves like a short circuit during its ON- state and acts as open circuit during its OFF-state. With this context explain the switching performance of BJT with relevant waveforms .Indicate clearly the turn –on and turn – off times and their components. [10 M]

   (C.O.NO.1) [Comprehension]

Part C (Problem Solving Questions)

Answer the Question. The Question carries ten marks. **(1Qx10M=10M)**

(C.O.NO.1) [Comprehension]

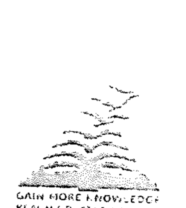
5. A bipolar junction transistor, with current gain beta=50 has a load resistance R_c= 10 ohms, DC supply voltage V_{cc}= 120V and input voltage to base circuit, V_B= 10 V. For V_{CES} = 1.2 V and V_{BES} = 1.6 V, Calculate

   (a) The value of R_B for operation in the saturated state

   (b) The value of R_B for an overdrive factor 6

   (c) Forced current gain

   (d) Power loss in the transistor for both parts (a) and (b)



SCHOOL OF ENGINEERING

Semester: V
Course Code: EEE 316
Course Name: **Power semiconductor devices (DE)**

Date: 30-9-2019
Time: 2:30PM-3:30PM
Max Marks: 40
Weightage: 20%

Extract of question distribution [outcome wise & level wise]

Q.NO	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels				Thought provoking type [Marks allotted] Bloom's Levels			Problem Solving type [Marks allotted]			Total Marks
			K				C			C			
PART-A	C.O.1 &2	Module1	1 -10 Q 10M (1 Mark each)										10M
PART B	C.O.1 &2	Module1					1 8 M	2 2 M	3 10M				20M
PART C	C.O.1 &2	Module1								1 10M			1 * 10 M 10M
	Total Marks												40M

K =Knowledge Level   C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt. About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

[I hereby certify that All the questions are set as per the above guide lines. Ramya N]

Reviewers' Comments

Annexure- II: Format of Answer Scheme

SCHOOL OF ENGINEERING

SOLUTION

Semester: V

Course Code: EEE 316

Course Name: **Power Semiconductor Devices**

Date: 30-9-2019

Time: 2:30 PM-3:30 PM

Max Marks: 40

Weightage: 20%

Part A (1 x 10 = 10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question

1	1-C	Objective type	1 min each
2	2-D		
3	3-D		
4	4-B		
5	5-D		
6	6-A		
7	7-A		
8	8-C		
9	9-C		
10	10-A		10 min

Part B (20M)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	Breakdown in diodes Avanlanche breakdown for > 7V and moderately doped Zener breakdown <5V and lightly doped Graphs of V versus I indicating breakdown voltages for various phenomenon.	• Understanding the breakdown phenomenon in diodes for different power rating and doping concentration (2M) • Explanation of Avalanche breakdown along with its breakdown characteristics (4M) • Explanation of Zener breakdown along with its breakdown characteristics (4M)	10 min
2	Cut in voltage for silicon diode and its definition Cut in voltage-can also be called as barrier potential , knee voltage	• Understanding the cut in voltage (1M) • Various synonyms of cut in voltage (1M)	2 min
3	Input characteristics in CE configuration Ib versus Vbe as a function of Vce Output characteristics in CE configuration Ic versus Vce as a function of Ib	• Circuit diagram and KVL analysis in CE mode (2M) • Draw the waveforms of input and output characteristic's in CE Mode. (4M) • Identifying the regions of saturation and cut off mode from output characteristics. (2M) • Explanation of early effect and current amplification in output characteristics (2M)	15 min

	For Vce<0 and for Vce=very small values -> Saturation region For Ib <0 BJT works in cut off mode		

Part C

(1x 10M = 10Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	(a) Rb=26.357ohms (b) Rb= 5.27 ohms (c) Forced beta= 8 (d) Power loss = 13.384W (e) Power loss=15.32W	• Circuit diagram in CE mode with KVL equations to input and output loop. (2M) • Computing the Rb for first case (2M) • Computing the Rb for second case(2M) • Computing forced beta (2M) • Power loss equation and calculation (2M)	15min

PRESIDENCY UNIVERSITY
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SCHOOL OF ENGINEERING

TEST –2

Sem & AY: Odd Sem 2019-20 | **Date**: 18.11.2019

Course Code: EEE 316 | **Time**: 2:30 PM to 3:30 PM

Course Name: POWER SEMICONDUCTOR DEVICES | **Max Marks**: 40

Program & Sem: BTech. (EEE) & V Sem | **Weightage**: 20%

Instructions:

I. *Read the question properly and answer accordingly.*
II. *Question paper consists of 3 parts.*
III. *Scientific and Non-programmable calculators are permitted.*

Part A [Memory Recall Questions]

Answer both the Questions. Each question carries five marks. (2Qx5M=10M)

1. What do you understand by latching and holding current of SCR. Denote the same in I-V characteristics of SCR. (C.O.NO.1)[Knowledge]
2. Explain with the help of diagram, the constructional features of IGBT. (C.O.NO.1)[Knowledge]

PART B [Thought Provoking Questions]

Answer all the Questions. (3Q=20M)

3. Justify the statement taking the help of V-I characteristics of SCR" higher the gate current, lower is the forward break over voltage". [7M](C.O.NO.1)[Comprehension]
4. In power MOSFET's ,the magnitude of drain current is a function of potential applied between drain and source terminals, In this context, discuss the output drain characteristics of power MOSFET's .Indicate the region of operation clearly. [8M](C.O.NO.1)[Comprehension]
5. With the increase in voltage between gate and source terminals, process of inversion initiates, and channel is formed especially in Enhancement type MOSFET. Explain How? [5M](C.O.NO.1)[Comprehension]

PART C [Problem Solving Questions]

Answer the Questions. The question carries ten marks. (1Qx10M=10M)

6. The SCR has the latching current of 50mA and is fired by the pulse width of 50 micro second.
   I. Determine whether the SCR triggers or not. The supply voltage applied is 100 V and the value of load resistance and inductance is 20 ohms and 0.5 H respectively. Draw the circuit diagram.
   II. Now if the latching current of the SCR is 4mA, find the minimum width of the gate trigger pulse required to properly turn on SCR.

(C.O.NO.1)[Comprehension]

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

Semester: V

Course Code: EEE 316

Course Name: **Power semiconductor devices (DE)**

Date: 18-11-2019

Time: 2:30PM-3:30PM

Max Marks: 40

Weightage: 20%

Extract of question distribution [outcome wise & level wise]

Q.NO.	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels				Thought provoking type [Marks allotted] Bloom's Levels			Problem Solving type [Marks allotted]			Total Marks
			K				C			C			
PART-A	C.O.1 &2	Module1	2*5 =10 Marks										**10M**
PART B	C.O.1 &2	Module1					1 7 M	2 8 M	3 5M				**20M**
PART C	C.O.1 &2	Module1								1 10M			**1 * 10 M** **10M**
	Total Marks												**40M**

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

Annexure- II: Format of Answer Scheme

SCHOOL OF ENGINEERING

SOLUTION

Semester: V

Course Code: EEE 316

Course Name: **Power Semiconductor Devices**

Date: 30-9-2019

Time: 2:30PM-3:30PM

Max Marks: 40

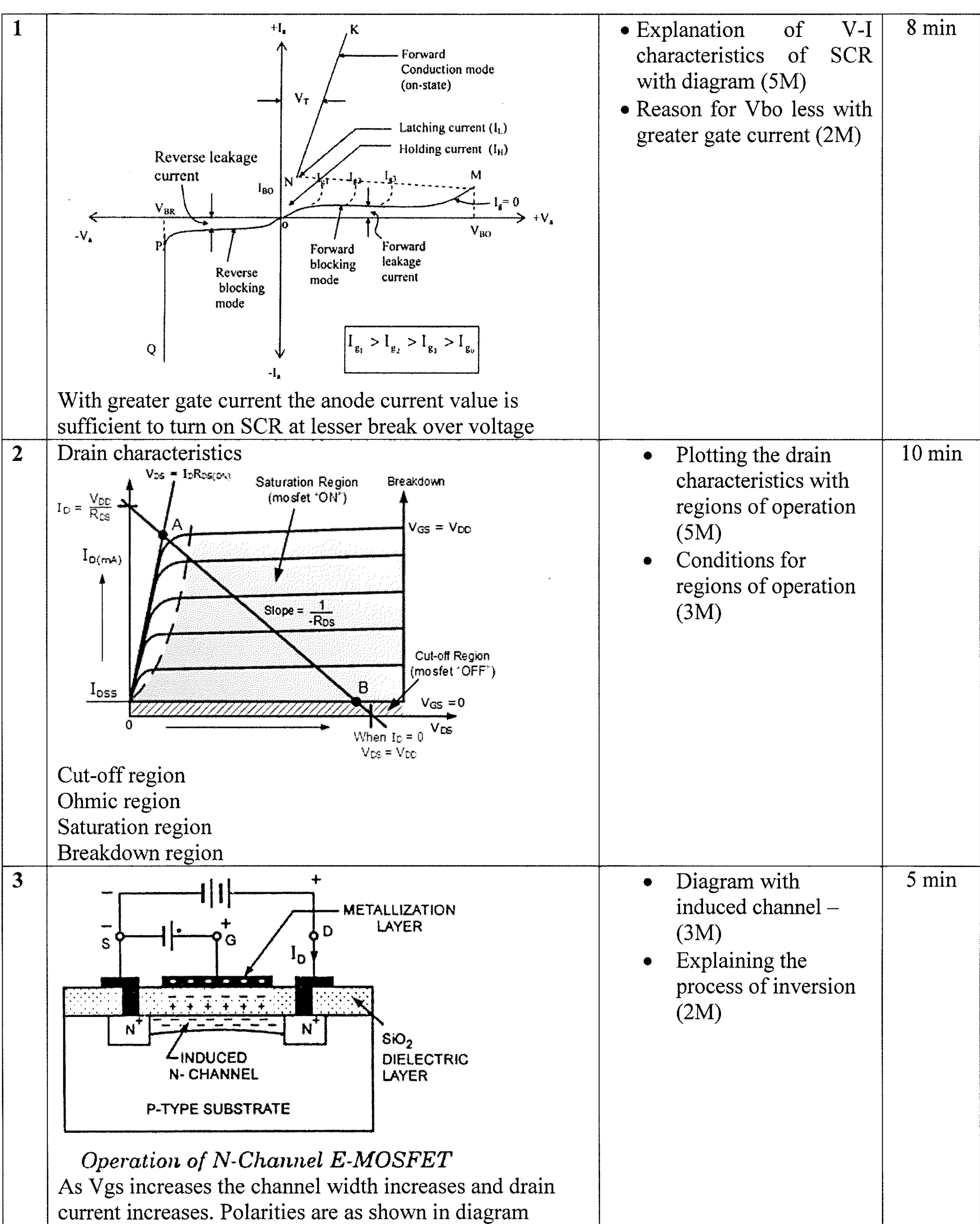
Weightage: 20%

Part A (1 x 10 = 10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	Latching current: Minimum forward current to keep SCR in conduction mode at the time of triggering (10-15)mA Holding Current : Minimum forward current to keep SCR in conduction mode (8-10)mA	• **Definition with range – 3M** • **Indicating on I-V characteristics – 2M**	
2	Constructional features of IGBT	**Diagram with P and N layers indicated -3M** **Explanation -2M**	10 min

Part B (20M)

Q No	Solution	Scheme of Marking	Max. Time required for each Question



1	With greater gate current the anode current value is sufficient to turn on SCR at lesser break over voltage	• Explanation of V-I characteristics of SCR with diagram (5M) • Reason for Vbo less with greater gate current (2M)	8 min
2	Drain characteristics Cut-off region Ohmic region Saturation region Breakdown region	• Plotting the drain characteristics with regions of operation (5M) • Conditions for regions of operation (3M)	10 min
3	*Operation of N-Channel E-MOSFET* As Vgs increases the channel width increases and drain current increases. Polarities are as shown in diagram	• Diagram with induced channel – (3M) • Explaining the process of inversion (2M)	5 min

Part C (1x 10M = 10Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	(a) I(t)= 10mA (b) t = 20 microseconds SCR wont be triggered as i(t) is less than latching current	• Circuit diagram. (2M) • Computing i(t) (3M) • Computing pulse width (3M) • Interpretation of result (2M)	15 min

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PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Semester: Odd Sem. 2019 - 20 | **Date**: 26 December 2019

Course Code: EEE 316 | **Time**: 9:30 AM to 12:30 PM

Course Name: POWER SEMICONDUCTOR DEVICES | **Max Marks**: 80

Program & Sem: B.Tech (EEE) & V | **Weightage**: 40%

Instructions:

Read the question properly and answer accordingly.
Question paper consists of 3 parts.
Scientific and Non-programmable calculators are permitted

Part A [Memory Recall Questions]

Answer all the Questions. Each Question carries 2 marks. (10Qx2M=20M)

1. Write the usual range of latching and holding current of SCR (C.O.No.2) [Knowledge]
2. What is knee voltage in diode? What are other terms used for cut-in voltage? (C.O.No.1) [Knowledge]
3. What is meant by depletion layer in P-N junction diodes? What is it depleted of? (C.O.No.1) [Knowledge]
4. Define beta and forced beta for BJT's. (C.O.No.2) [Knowledge]
5. Define turn on and turn off times of SCR. (C.O.No.2) [Knowledge]
6. Give any two examples of voltage and current controlled devices. (C.O.No.1,2) [Knowledge]
7. What is the difference between enhancement and depletion type MOSFET's. (C.O.No.3) [Knowledge]
8. What do you understand by switching characteristics of any semiconductor device? (C.O.No.1,3) [Knowledge]
9. Write any 4 protection schemes for Thyristor. (C.O.No.4) [Knowledge]
10. What is Safe Operating Areas? What is its significance? (C.O.No.3) [Knowledge]

Part B [Thought Provoking Questions]

Answer all the Questions. Each Question carries 5 marks. (4Qx5M=20M)

11. BJT is essentially a back to back connected p-n junction diodes. Hence their input and output characteristics are closely linked with forward and reverse bias characteristics of p-n junction diodes. In this context, describe the output characteristics of BJT in Common Emitter mode. Show the region of transistor characteristics where it acts like a switch (C.O.No.1,2) [Comprehension]
12. The SCR has the latching current of 30mA and is fired by the pulse width of 50 micro second. Determine whether the SCR triggers or not. The supply voltage applied is 100 V and the value of load resistance and inductance is 20 ohms and 0.5 H respectively. Draw the circuit diagram. (C.O.No.2,3) [Comprehension]

13. In power MOSFET's, the magnitude of I_D depends on V_{GS}, in this context, sketch and discuss how the drain current and drain to source voltage varies as a function of input voltage V_{GS}. (C.O.No.1, 2) [Comprehension]
14. How does the process of induced channel take place in Enhancement type MOSFET? Explain (C.O.No.2) [Comprehension]

Part C [Problem Solving Questions]

Answer all the Questions. Each Question carries 10 marks. (4Qx10M=40M)

15. (a) With the help of two transistor model explain how GTO can be turned off?
    (b) How does the anode shorted GTO help in speeding up of turn off process.

    (C.O.No.2,3) [Comprehension]
16. Explain why latch up problems are prevalent in IGBT's, support your answers with the structure of IGBT indicating the different biasing potentials.
    (C.O.No.2,3) [Comprehension]
17. (a) With the help of RC snubber circuit, explain how the false turn-on of a thyristor due to large dv/dt can it be prevented .
    (b) A SCR circuit operates from 300V DC supply, has series inductance of 4 micro Henry. A resistance of 4 ohms and capacitance of 0.2 Microfarad is connected across the SCR.Calculate the safe dv/dt and di/dt ratings of SCR.
    (C.O.No.4) [Comprehension]
18. Calculate the required parameters for snubber circuit to provide dv/dt protection to a SCR used in a single phase bridge converter. The SCR has a maximum dv/dt capability of 50 V/Microsecond. The input line to line voltage has a peak value of 325 V and the source inductance is 0.3 H. (C.O.No.4) [Comprehension]

SCHOOL OF ENGINEERING

GAIN MORE KNOWLEDGE REACH GREATER HEIGHTS

Semester: V

Course Code: EEE 316

Course Name: **Power semiconductor devices (DE)**

Date: 26-12-2019

Time: 9:30AM-12:30PM

Max Marks: 80

Weightage: 40%

Extract of question distribution [outcome wise & level wise]

Q.NO.	C.O.NO (% age of CO)	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	C	
1	1,2	2	2M			2
2	1	1	2M			2
3	1	1	2M			2
4	1,2	2	2M			2
5	1,2	2	2M			2
6	2,3	3	2M			2
7	1,2	2	2M			2
8	1,2	2	2M			2
9	3,4	4	2M			2
10	2,3	3	2M			2
11	1	1		5M		5
12	1,2	2		5M		5
13	2,3	3		5M		5

14	2,3	3		5M		5
15	2,3	3	10M			10
16	2,3	3	10M			10
17	3,4	4			10M	10
18	3,4	4			10M	10
			40	20	20	80

Total =80

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

I hereby certify that all the questions are set as per the above guidelines.

Faculty Signature:

Reviewer Commend:

Annexure- II: Format of Answer Scheme

SCHOOL OF ENGINEERING

SOLUTION

Semester: V

Course Code: EEE 316

Course Name: **Power Semiconductor Devices**

Date: 26-12-2019

Time: 9:30AM-12:30PM

Max Marks: 80

Weightage: 40%

Part A (2 x 10 = 20 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	Latching current: Minimum forward current to keep SCR in conduction mode at the time of triggering (10-15)mA Holding Current : Minimum forward current to keep SCR in conduction mode (8-10)mA	**1x2=2 M each**	30 min
2	The forward voltage at which the current through the junction starts increasing rapidly, is called the knee voltage or cut-in voltage.		
3	**Depletion region** or **depletion layer** is a **region** in a P-N junction diode where no mobile charge carriers are present. **Depletion layer** acts like a barrier that opposes the flow of electrons from n-side and holes from p-side.		
4.	Forced Beta or beta forced is typically used to describe a BJT that is operated as a switch in saturation (Vce << Vbe) Beta: A Bipolar Junction Transistor (BJT) when operated with DC inputs, the levels of its collector current *Ic* and base current *Ib* are related by the term *beta (β)*		

5.	Voltage controlled devices: IGBT and MOSFET Current controlled devices: SCR and BJT		
6.	In **Enhancement MOSFET**, the **channel** does not exist initially and is induced i.e the **channel** is developed by applying a voltage greater than threshold voltage, at the gate terminals. On the other hand, in **depletion MOSFET**, the **channel** is permanently fabricated (by doping) at the time of construction of **MOSFET** itself.		
7.	**Turn off time of SCR** :can be defined as the interval between anode current falls to zero and device regains its forward blocking mode **Thyristor turn on time** may be defined as the **time** required by the **SCR** to change its state from forward blocking mode to forward conduction mode when a gate pulse is applied.		
8.	It is the time variation of voltage across its anode and cathode terminals and the current through it during its turn on and turn off process		
9.	(a) dv/dt protection (b) Over voltage protection (c) Over current protection (d) di/dt protection		
10.	For power semiconductor devices (such as BJT, MOSFET, thyristor or IGBT), the *safe operating area* (SOA) is defined as the voltage and current conditions over which the device can be expected to operate without self-damage		

Part B (4x5=20M)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
11	Input characteristics in CE configuration Ib versus Vbe as a function of Vce Output characteristics in CE configuration Ic versus Vce as a function of Ib For Vce<0 and for Vce=very small values -> Saturation region For Ib <0 BJT works in cut off mode	• Draw the waveforms of input and output characteristic's in CE Mode. (3M) • Identifying the regions of saturation and cut off mode from output characteristics. (2M)	7 min
12	(a) I(t)= 10mA	• Circuit diagram. (2M) • Computing i(t) (3M)	7 min
13	Drain characteristics Saturation Region (mosfet ON) · Breakdown · $V_{GS} = V_{DD}$ · $I_{D(mA)}$ · Slope = $\frac{1}{-R_{DS}}$ · Cut-off Region (mosfet "OFF") · I_{DSS} · A · B · $V_{GS} = 0$ · V_{DS} · 0 Cut-off region Ohmic region Saturation region Breakdown region	• Plotting the drain characteristics with regions of operation (2M) • Conditions for regions of operation (3M)	10 min
14	METALLIZATION LAYER · S · G · D · I_D · N^+ · N^+ · INDUCED N- CHANNEL · SiO_2 DIELECTRIC LAYER · P-TYPE SUBSTRATE *Operation of N-Channel E-MOSFET* As Vgs increases the channel width increases and drain current increases. Polarities are as shown in diagram	• Diagram with induced channel –(3M) • Explaining the process of inversion (2M)	10 min

Part C (4x 10M = 40Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
15	$\Rightarrow -I_g' < \frac{I_a}{\alpha_2}(1-\alpha_2) - I_a\alpha_1\left[1+\frac{1-\alpha_2}{\alpha_2}\right]$ $-I_g' < I_a\left(\frac{1}{\alpha_2}-1\right) - I_a\left(\frac{\alpha_1}{\alpha_2}\right)$ $I_g' > I_a\left[\frac{\alpha_1}{\alpha_2} - \left(\frac{1}{\alpha_2}-1\right)\right]$ $\boxed{I_g' > I_a\left(\frac{\alpha_1+\alpha_2-1}{\alpha_2}\right)}$ $\Rightarrow k = \frac{\alpha_1+\alpha_2-1}{\alpha_2}$	• Circuit diagram of two transistor model. (3M) • Expression of Ig (3M) • Diagram and explanation of anode shorted GTO (3M) • Interpretation of result (1M)	15 min
16	1. Vertical cross section of an IGBT showing the on-state current flow paths 3. More complete IGBT equivalent circuit showing the transistors Comprising the parasitic thyristor	• Circuit diagram of IGBT (3M) • Two transistor model explanation(3M) • Latch up problem (3M) • Avoiding latch up problems (1M)	15 min
17(a)	R C SCR	• Diagram of RC Snubber (2M) • Explanation with design values (3M)	7 min

(b)	di/dt = 75A/Microsecond dv/dt = 133.76 V/Microsecond	• di/dt calculation (2M) • dv/dt calculation (2M) • Circuit with design values (1M)	6 min
18	C_s = 0.04 Micro Farad R_s = 92 ohms L_s = 0.5 H	• Formula with calculation C_s (3M) • Formula with calculation R_s (3M) • Formula with calculation L_s (3M) • Circuit with designed values (1M)	12 min