Roll No.													

PRESIDENCY UNIVERSITY
BENGALURU
SCHOOL OF ENGINEERING

TEST 1

Sem & AY: Odd Sem. 2019-20 | **Date**: 01.10.2019

Course Code: ECE 215 | **Time**: 1:00PM to 2:00PM

Course Name: VLSI DESIGN | **Max Marks**: 40

Program & Sem: B.Tech. (ECE) & VII | **Weightage**: 20%

Instructions:

i. Answer all the Questions.

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries two marks. (5Qx2M=10M)

1. What are the different levels of Design Description?
2. Define Data Flow style of modeling?
3. What is HDL? Name some HDLs?
4. Write the operator symbols for Bitwise logical operators?
5. Write the syntax for 2 types of Tristate Inverters?

[Q.No.1 to 5] (C.O.NO.1) [Knowledge]

Part B [Thought Provoking Questions]

Answer all the Questions. Each question carries five marks. (3Qx5M=15M)

6. What is contention? Demonstrate with a Verilog Module?
7. Write a Verilog Module and Test Bench for half adder in Structural style?
8. Write a Verilog Module and Test bench for 2X1 MUX using Ternary Operator?

[Q.No.6 to 8] (C.O.NO.1) [Comprehension]

Part C [Problem Solving Questions]

Answer the Question. The Question carries fifteen marks. (1Qx15M=15M)

9. Explain Design flow with a neat sketch? Write a Verilog module and Test Bench for UPCOUNTER in behavioral style? (C.O.NO.1) [Comprehension]

SCHOOL OF-ENGINEERING

Semester: 7

Course Code: ECE 215

Course Name: VLSI Design

Date: 01-10-2019

Time: 1 hour

Max Marks:40

Weightage: 20%

Extract of question distribution [outcome wise & level wise]

Q.NO.	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	A	
1-5	CO 1	Module 1	10			10
1-3	CO 1	Module 1		5 5 5		15
1	CO 1	Module 1		10	15	15
	Total Marks					40

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

[I hereby certify that All the questions are set as per the above guide lines. Mr. Vijaya Krishna]

Reviewers' Comments

(1) The QP has been set exactly for 60 minutes. At least 05 minutes should be given for reading the Q.P.

(2) For Part 'c', expected solution seems lengthy as per the marks assigned.

Annexure- II: Format of Answer Scheme

SCHOOL OF ENGINEERING

SOLUTION

Semester: 7

Course Code: ECE 215

Course Name: VLSI Design

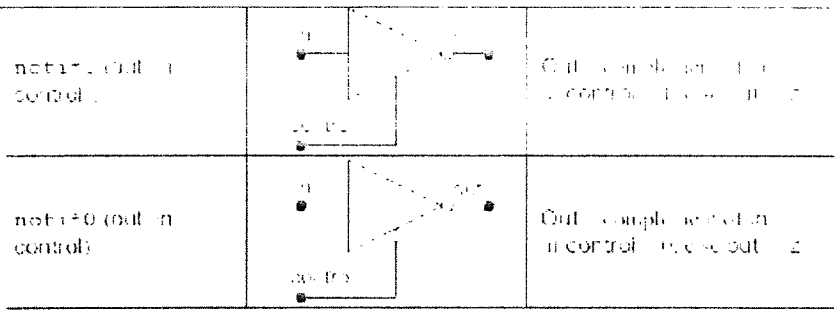
Date 01-10-2019

Time: 1 hour

Max Marks:40

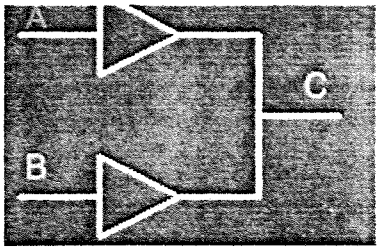
Weightage 20%

Part A (5Q x 2M = 10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	Structural, Dataflow, Behavioral	2	2
2	Data Flow is defined as set of concurrent statements.	2	2
3	Hardware Description Language. VHDL and Verilog	2	2
4	AND & OR | XOR ^ XNOR ~^	2	2
5		2	2

Part B (3Q x 5M = 15Marks)

Q No	Soiution	Scheme of Marking	Max. Time required for each Question
1	If a wire takes two different values from different sources then contention arises. A single wire cannot hold two values at a time. To avoid contention nets are given with different strengths. Module contres(c,a,b); Input a,b; Output c; buf (supply1, pull0) g1(c,a),g2(c,b); endmodule	2+2+1=5	5

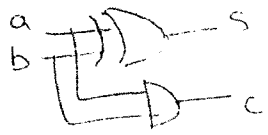


2

3-2-5

5

Half adder:



a	b	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Module

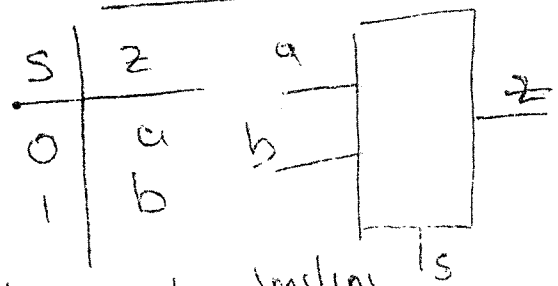
```
timescale 1ns/1ns;
module Ha(s,c,a,b);
 output s,c;
 input a,b;
 xor x1(s,a,b);
 and a1(c,a,b);
 endmodule
```

```
`timescale 1ns/1ns
module half_tb();
wire s,c;
reg a,b;
half_adder ha1(s,c,a,b);
initial begin
a=0; b=0;
#2 a=0; b=1;
#3 a=1; b=0;
#4 a=1; b=1;
#10 $stop;
end
endmodule
```

3

2x1 MUX module

S	Z
0	a
1	b




```
`timescale 1ns/1ns
module mux21(z,a,b);
output z;
input a,b;

assign z=(s==0)?a:b;

endmodule
```

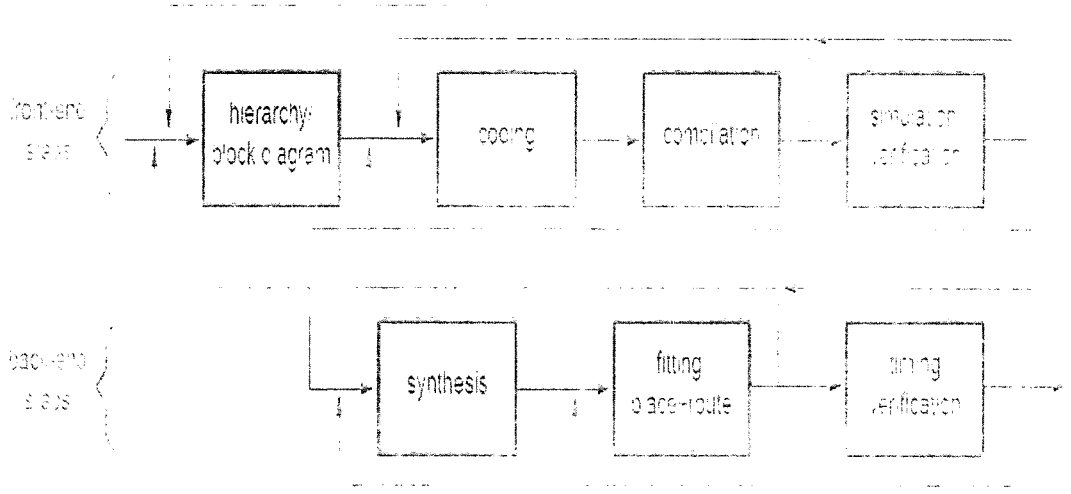
3+2=5

5

```
module mux2_tb();
wire z;
reg s,a,b;
mux2_1 m1(z,a,b);
 initial begin
    s=0; a=0; b=0;
 #2 s=0; a=0; b=1;
 #4 s=1; a=1; b=0;
 #10 $stop;
  end
 endmodule
```

Part C (1Q x 10M = 10Marks)

No	Solution	me of Mark ing	Time required for each Question
1	**Design Flow:** There are several steps in a VHDL-based design process, often called the design flow.	10+3+2=15	35



Hierarchy/Block Digram

The "front end" begins with figuring out the basic approach and building blocks at the block diagram level. Large logic designs, like software programs, are usually hierarchical, and VHDL gives us a good framework for defining modules and their interfaces, and filling in the details.

Coding:

The actual writing of VHDL code for modules, their interfaces, and their internal details. VHDL is a text-based language, in principle you can use any text editor for this part.

A specialized VHDL text editor include features like automatic highlighting of VHDL keywords, automatic indenting, built-in templates for frequently used program structures, and built-in syntax checking and one-click access to the compiler.

Compiler:

A VHDL compiler analyzes your code for syntax errors and also checks your code for compatibility with other modules on which it relies

It also creates the internal information that is needed for a simulator to process your design later. As in other programming endeavors, you probably shouldn't wait until the very end of coding to compile all of your code.

Doing a piece at a time can prevent you from proliferating syntax errors, inconsistent

Simulator:

A VHDL simulator allows you to define and apply inputs to your design, and to observe its outputs, without ever having to build the physical circuit.

In small projects we would probably generate inputs and observe outputs manually But for larger projects, VHDL gives you the ability to create "test benches" that automatically apply inputs and compare them with expected outputs.

There are two types of verification

1) Functional Verification
2) Timing Verification

In functional verification, we study the circuit's logical operation independent of timing considerations; gate delays and other timing parameters are considered to be zero.

In timing verification, we study the circuit's operation including estimated delays, and we verify that the setup, hold, and other timing requirements for sequential devices like flip-flops are met. Functional verification before starting the back-end steps.

In back-end there are three basic steps

1) Synthesis 2)Fitting Place + Route 3) Timing Verification

Synthesis:

The synthesis, converting the VHDL description into a set of primitives or components that can be assembled in the target technology.

For example, with PLDs or CPLDs, the synthesis tool may generate two-level sum-of-products equations.In the fitting step, a fitting tool or fitter maps the synthesized primitives or components onto available device resources.

Place & Route:

For a PLD or CPLD, this may mean assigning equations to available AND-OR elements. For an ASIC, it maymean laying down individual gates in a pattern and finding ways to connect them within the physical constraints of the ASIC die.The "final" step is timing verification of the fitted circuit. Actual circuit delays due to wire lengths, electrical loading, and other factors can be calculated with reasonable precision.

```
module  count_up(clk, clr, N);
  input clk;
  input [3:0] N;
  output [3:0]a;
  reg [3:0] a;
  initial  a= 4'b 0000;
  always @ (negedge clk)
     a= (a==N)? 4'b0000 : a+1'b1;
  endmodule.

module  tst_count_up;
  reg clk;
  reg [3:0] N;
  wire [3:0]a;
  count_up C1(a, clr, N);
  initial
    begin
        clk=0;
        N = 4'b 1011;
  end
  always #2  clk= ~clk;
  endmodule.
```

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TEST – 2

Sem & AY: Odd Sem 2019-20 | **Date:** 19.11.2019

Course Code: ECE 215 | **Time:** 1.00 PM to 2.00 PM

Course Name: VLSI DESIGN | **Max Marks:** 40

Program & Sem: Btech. (ECE) & VII Sem | **Weightage:** 20%

Instructions:

(i) Read Questions carefully and answer accordingly.

(ii) Scientific and Non- programmable calculators are permitted.

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries two marks. (5Qx2M=10M)

(C.O.NO.2&3)[Knowledge]

1. Define Moore's Law?
2. Write the Expression for Trans-conductance?
3. What is Lithography?
4. Which layers are used for forming PMOS transistor?
5. Draw the stick encoding for Implant and write its color?

Part B [Thought Provoking Questions]

Answer all the Questions. Each question carries five marks. (3Qx5M=15M)

(C.O.NO.3)[Comprehension]

6. Explain NMOS Inverter with circuit diagram?
7. Draw the Layout for 3 input NMOS NAND gate with color representation?
8. Explain Lambda based design rules for Wires and Transistors?

Part C [Problem Solving Questions]

Answer the Question. The question carry fifteen marks. (1Qx15M=15M)

9. Derive the Expression for Ids (drain to source current) of MOS transistor in Non-Saturation and Saturation regions? (C.O.NO.2)[Comprehension]

SCHOOL OF-ENGINEERING

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

Semester: 7
Course Code: ECE 215
Course Name: VLSI Design

Date: 19-11-2019
Time: 1 hour
Max Marks:40
Weightage: 20%

Extract of question distribution [outcome wise & level wise]

Q.NO	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels			Thought provoking type [Marks allotted] Bloom's Levels			Problem Solving type [Marks allotted]			Total Marks
			K			C			A			
1-5	CO 2 CO 3	Module 2 Module 3	10									10
1-3	CO 3	Module 3				5	5	5				15
1	CO 2	Module 2							15			15
	Total Marks											40

Reviewer's Comments :-

(1) Questions are well planned, however following observations I have :-

- Thought provoking questions are replaced with explanation based questions.
- Problem Solving Type question contains a derivation. Small portion of evaluation could have been included.

Rsingh
14/11/19

Annexure- II: Format of Answer Scheme

SCHOOL OF ENGINEERING

SOLUTION

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

Semester: 7

Course Code: ECE 215

Course Name: VLSI Design

Date:19-11-2019

Time: 1 hour

Max Marks:40

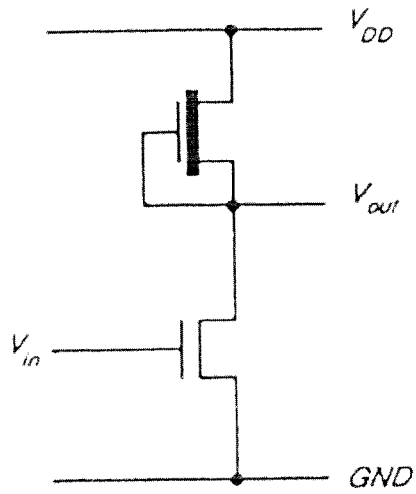
Weightage: 20%

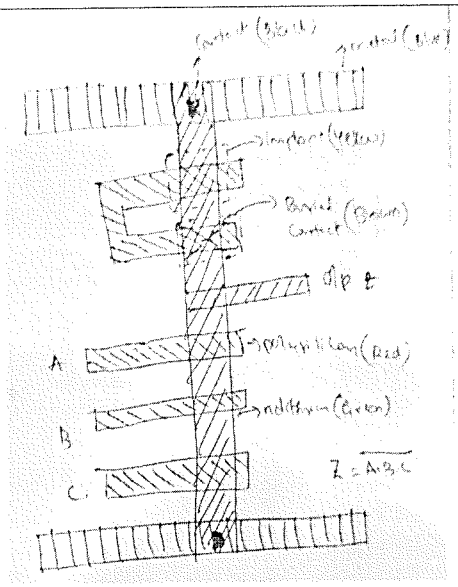
Part A (5Q x 2M = 10 Marks)

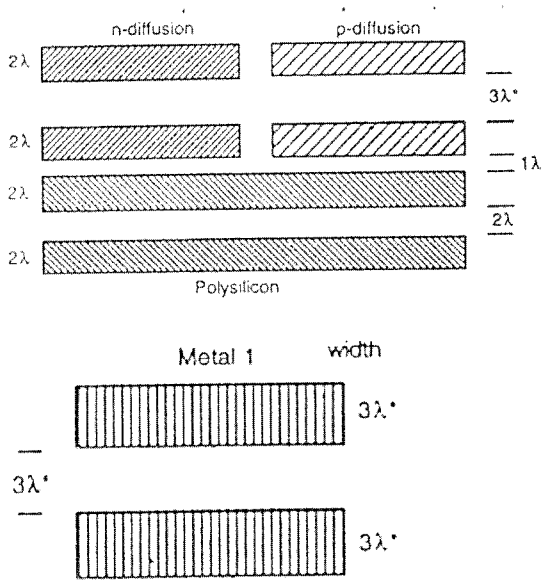
Time for reading question paper 5 Min

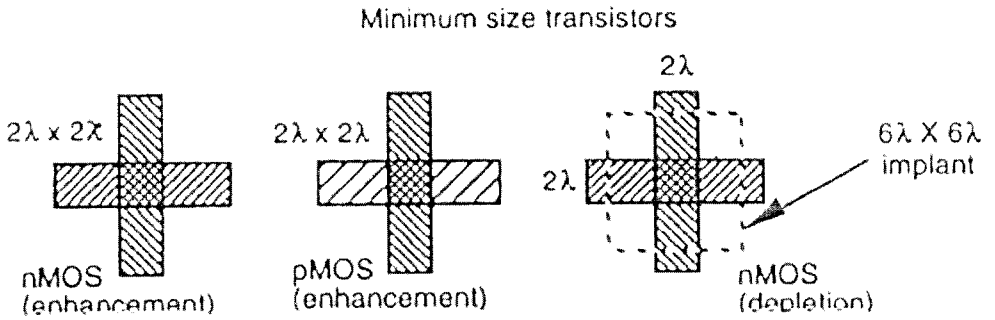
Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	The number of transistors doubled approximately every 18 months.	2	2
2	$g_m = \frac{\mu \varepsilon_{ins} \varepsilon_0}{D} \frac{W}{L} (V_{gs} - V_t)$	2	2
3	It is used to pattern specific shapes of a thin layer on a rigid substrate for fabricating electrical devices. These devices are the result of direct and monolithic integration of several layers on a wafer.	2	2
4	Poly silicon and P diffusion	2	2
5	 **Yellow**	2	2

Part B (3Q x 5M = 15Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	 With no current drawn from the output, the currents I_{ds} for both transistors must be equal. • For the depletion mode transistor, the gate is connected to the source so it is always on and only the characteristic curve V_{gs} = 0 is relevant. • In this configuration the depletion mode device is called the pull-up (p.u.) and the enhancement mode device the pull-down (p.d.) transistor. • To obtain the inverter transfer characteristic we superimpose the V_{gs} = 0 depletion mode characteristic curve on the family of curves for the enhancement mode device, noting that maximum voltage across the enhancement mode device corresponds to minimum voltage across the depletion mode transistor. • The points of intersection of the curves as in Figure *f-6* give points on the transfer characteristic, which is of the form shown in Figure 2.7. • Note that as V_{in}(=V_{gs} p.d. transistor) exceeds the p.d. threshold voltage current begins to flow. The output voltage V_{out} thus decreases and the subsequent increases in V_{in} will cause the p.d. transistor to come out of saturation and become resistive. Note that the p.u. transistor is initially resistive as the p.d. turns on.	2+3=5	5
2		5	5


A
B
C
Z = A B C

3	 n-diffusion p-diffusion 2λ 2λ 2λ 2λ 3λ* 1λ 2λ Polysilicon Metal 1 width 3λ* 3λ* 3λ*	3+2=5	5



Part C (1Q x 15M = 15Marks)

Q No	Solution	Scheme of Mark	Max. Time require

		ing	d for each Question
1	$$I_{ds} = -I_{sd} = \frac{\text{Charge induced in channel } (Q_c)}{\text{Electron transit time } (\tau)}$$ First, transit time: $$\tau_{sd} = \frac{\text{Length of channel } (L)}{\text{Velocity } (v)}$$ but velocity $$v = \mu E_{ds}$$ where μ = electron or hole mobility (surface) E_{ds} = electric field (drain to source) Now $$E_{ds} = \frac{V_{ds}}{L}$$ so that $$v = \frac{\mu V_{ds}}{L}$$ Thus $$\tau_{sd} = \frac{L^2}{\mu V_{ds}}$$ Typical values of μ at room temperature are: $\mu_n \doteq 650$ cm^2/V sec (surface) $\mu_p \doteq 240$ cm^2/V sec (surface) **The Non-saturated Region**	15	30

Note that the charge/unit area = $E_g \varepsilon_{ins} \varepsilon_0$. Thus induced charge

$$Q_c = E_g \varepsilon_{ins} \varepsilon_0 WL$$

where

E_g = average electric field gate to channel
ε_{ins} = relative permittivity of insulation between gate and channel
ε_0 = permittivity of free space

(*Note*: $\varepsilon_0 = 8.85 \times 10^{-14}$F cm^{-1}; $\varepsilon_{ins} \doteq 4.0$ for silicon dioxide)

Now

$$E_g = \frac{\left((V_{gs} - V_t) - \frac{V_{ds}}{2} \right)}{D}$$

where D = oxide thickness.

Thus

$$Q_c = \frac{WL\varepsilon_{ins}\varepsilon_0}{D} \left((V_{gs} - V_t) - \frac{V_{ds}}{2} \right)$$

Now, combining equations (2.2) and (2.3) in equation (2.1), we have

$$I_{ds} = \frac{\varepsilon_{ins}\varepsilon_0 \mu}{D} \frac{W}{L} \left((V_{gs} - V_t) - \frac{V_{ds}}{2} \right) V_{ds}$$

The factor W/L is, of course, contributed by the geometry and it is common practic write

$$\beta = K \frac{W}{L}$$

or

$$I_{ds} = K \frac{W}{L} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

in the non-saturated or resistive region where $V_{ds} < V_{gs} - V_t$ and

$$K = \frac{\varepsilon_{ins}\varepsilon_0 \mu}{D}$$

so that

$$I_{ds} = \beta\left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

which is an alternative form of equation (2.4).

Noting that gate/channel capacitance

$$C_g = \frac{\varepsilon_{ins}\varepsilon_0 WL}{D} \text{ (parallel plate)}$$

we also have

$$K = \frac{C_g \mu}{WL}$$

so that

$$I_{ds} = \frac{C_g \mu}{L^2} \left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

The Saturated Region

Saturation begins when $V_{ds} = V_{gs} - V_t$ since at this point the *IR* drop in the channel ec the effective gate to channel voltage at the drain and we may assume that the current rem fairly constant as V_{ds} increases further. Thus

$$I_{ds} = K \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2}$$

$$I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2$$

$$I_{ds} = \frac{C_g \mu}{2L^2} (V_{gs} - V_t)^2$$

$$I_{ds} = C_0 \mu \frac{W}{2L} (V_{gs} - V_t)^2$$

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SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Semester: Odd Semester: 2019 - 20 | **Date**: 28 December 2019

Course Code: ECE 215 | **Time**: 9:30 AM to 12:30 PM

Course Name: VLSI DESIGN | **Max Marks**: 80

Program & Sem: B.Tech (ECE) & VII | **Weightage**: 40%

Instructions:

(i) Read the all questions carefully and answer accordingly.
(ii) Scientific and Non- programmable calculators are permitted
(iii) This question paper contains Two pages

Part A [Memory Recall Questions]

Answer all the Questions. Each Question carries 2 marks. (10Qx2M=20M)

(C.O.No.1-5) [Knowledge]

1. What is Synthesis and Simulation?
2. Define Data Flow style of modeling?
3. Write the equation for Figure of Merit?
4. Define Body effect in NMOS device?
5. Draw the Stick encoding for Polysilicon and write its color?
6. Write the condition for NMOS transistor to be in Non-Saturation region?
7. Name three dynamic logics used to deign digital circuits?
8. How many address lines and data lines are required for 8X4 ROM?
9. Write the expression for voltage gain for Common Drain configuration?
10. Draw the basic circuit for Common Source configuration?

Part B [Thought Provoking Questions]

Answer all the Questions. Each Question carries 4 marks. (5Qx6M=30M)

[Comprehension]

11. Write a Verilog Module and Test Bench for 4X1 MUX in Dataflow style? (C.O.No.1)
12. Draw the Circuit and Stick Diagram for CMOS OAI gate with color representation? (C.O.No.3)
13. Design 8X4 ROM using MOS Transistors with necessary truth table? (C.O.No.4)
14. Design SRAM Memory for storing 8 bits of data in 4 memory locations using SRAM Cells? (C.O.No.4)

15. Design the circuit for the following function in Dynamic CMOS logic?

(C.O.No.4)

$$Z = \overline{A + (B.C)}$$

Part C [Problem Solving Questions]

Answer both the Questions. Each Question carries 15 marks. **(2Qx15M=30M)**

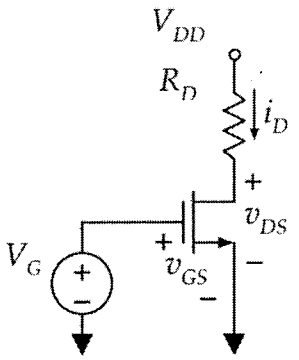
[Application]

16. A) Explain the operation of CMOS Inverter with neat sketch? (C.O.No.2)

B) For the below circuit find I_D and V_{DS}? In which region the transistor is operating? Justify

V_t=1.5v, $\beta = 1$, V_g=4v, V_{dd}=5v, R_D=1 K ohm

(C.O.No.2)



17. A) Draw the Basic Current Mirror circuit and write the equation for I_{ref}

(C.O.No.5)

B) An Enhancement PMOS transistor has $\beta = \frac{80\mu A}{V^2}$, Vt=-1.5V, $\lambda = -0.02\,V^{-1}$. The Gate is connected to ground and the source to 5 V. Find the Drain current for Vd=0V and -5V

(C.O.No.5)

GAIN MORE KNOWLEDGE
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SCHOOL OF ENGINEERING

END TERM FINAL EXAMINATION

Extract of question distribution [outcome wise & level wise]

Q.NO.	C.O.NO (% age of CO)	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels K	Thought provoking type [Marks allotted] Bloom's Levels C	Problem Solving type [Marks allotted] A	Total Marks
PART A						
1-2	1	1	4			
3-4	2	2	4			
5-6	3	3	4			20
7-8	4	4	4			
9-10	5	5	4			
PART B						
1	1	1		6		
2	3	3		6		
3	4	4		6		30
4	4	4		6		
5	4	4		6		
PART C						
1	2	2	5		10	30
2	5	5	5		10	
	Total Marks		30	30	20	80

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

I hereby certify that all the questions are set as per the above guidelines.

Faculty Signature:

Reviewer Comment:

Everything O.K. except Part B (Thought Provoking Questions). Faculty member has to comply next Sem. onwards.

Format of Answer Scheme

SCHOOL OF ENGINEERING

SOLUTION

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

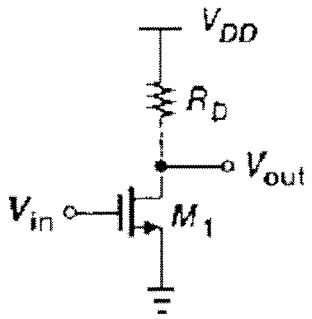
Semester: Odd Sem. 2019-20
Course Code: ECE215
Course Name: VLSI Design
Program & Sem: B.Tech & 7Th

Date: 28.12.2019
Time: 3 HRS
Max Marks: 80
Weightage: 40%

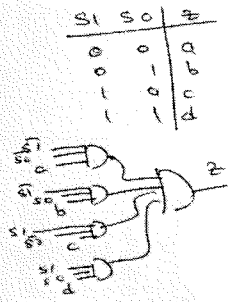
Part A (10Q x 2M = 20Marks)

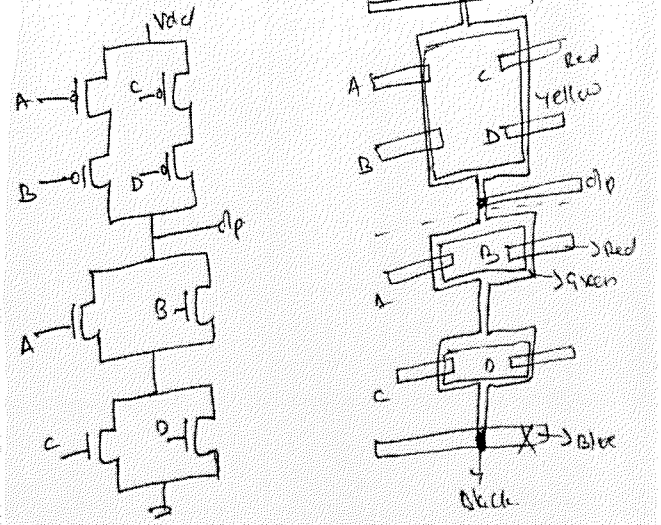
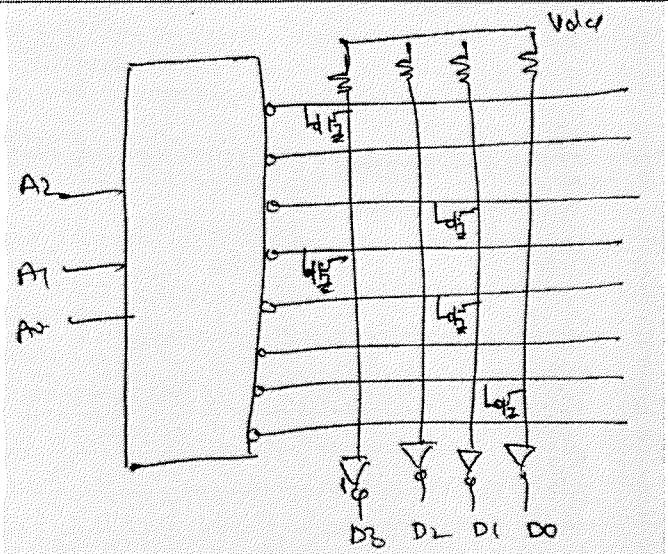
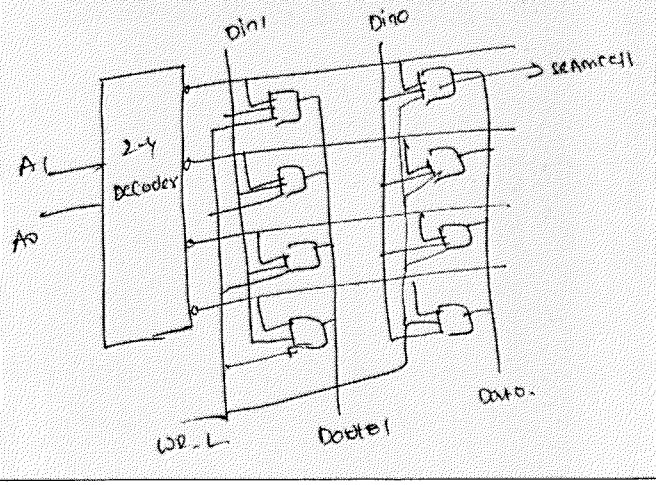
5 Minutes for reading Question Paper

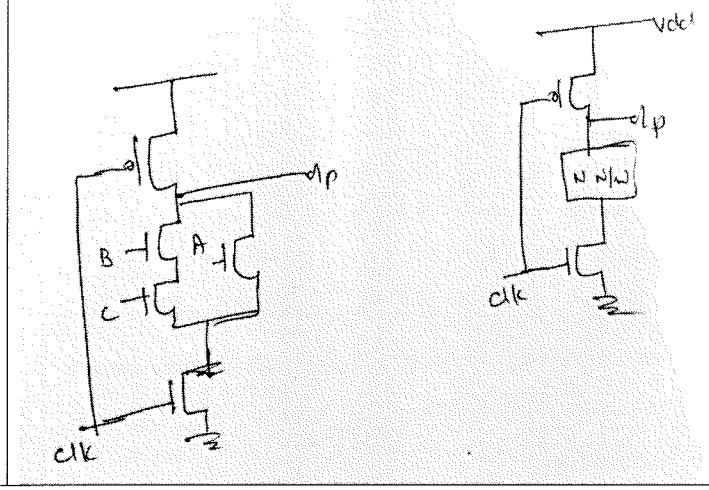
Q No	Solution	Scheme of Marking	Max. Time required for each Question (MIN)
1	Generating gate level netlist is called synthesis, Functional verification of a design is called simulation	2	2
2	Dataflow is defined as set of concurrent statements	2	2
3	$\omega_0 = \frac{g_m}{C_g} = \frac{\mu}{L^2}(V_{gs} - V_t)\left(= \frac{1}{\tau_{sd}}\right)$	2	2
4	The *body effects* may also be taken into account since the substrate may be biased with respect to the source Increasing V_{SB} causes the channel to be depleted of charge carriers and thus the threshold voltage is raised. Change in V_t is given by $\Delta V_t \doteq \gamma(V_{SB})^{1/2}$ where γ is a constant which depends on substrate doping so that the more lightly doped the substrate, the smaller will be the body effect.	2	2
5	RED  Polysilicon	2	2
6	$V_{gs} > V_t$ $V_{ds} < V_{gs} - V_t$	2	2
7	Dynamic CMOS, Clocked CMOS, CMOS Domino Logic	2	2
8	3,4	2	2
9	$A_v = \frac{g_m R_S}{1 + (g_m + g_{mb})R_S}$	2	2

10		2	2

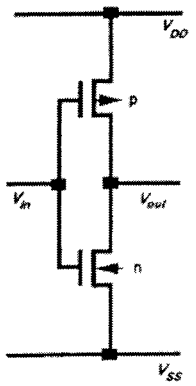
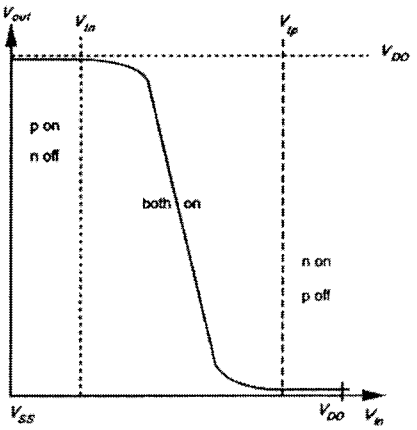
Part B (5Q x 6M = 30 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	 Module `timescale 1ns/1ns; module mux(z,s,a,b,c,d); output z; input [1:0] s; input a,b,c,d; assign z=(~s1 && ~s0 && a) || (~s1 && s0 && b) || (s1 && ~s0 && c) || (s1 && s0 && d); endmodule. Test Bench: `timescale 1ns/1ns; module mux_tb(); wire z; reg a,b,c,d,s; mux m1(z,s,a,b,c,d); initial begin s=00 a=0; b=1; c=0; d=1; #2 s=2'b01; #10 $stop; end endmodule.	½+1/2+3+2	20

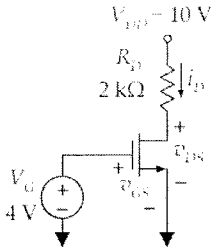
2	CAI gate: $Z = \overline{(A+B)\cdot(C+D)}$ 	3+3	20
3		2+3+1	15
4	SRAM: 4 memory locations 8 bits 	2+3+1	15

5	$Z = \overline{A+(B.C)}$ in dynamic CMOS logic 	1+1+4	15

Part C (2Q x 15M = 30Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	(a) No current flow either for logical 0 or for logical 1 inputs. (b) Full logical 1 and 0 levels are presented at the output. (c) For devices of similar dimensions the p-channel is slower than the n-channel device.  (a) Circuit  (b) Transfer characteristic	2+4+3+3+3	35

For the circuit shown, use the the NMOS equations to find i_D and v_{DS}.



For the NMOS, V_T = 1.5 V and K = 0.5 mA/V².

$v_{GS} = V_G = 4$ V → the NMOS is on.

Assume that the transistor is in saturation.

$$i_D = K(v_{GS} - V_T)^2 = \left(0.5\text{mA/V}^2\right)[4\text{V} - 1.5\text{V}]^2 = 3.125\text{mA}$$

$$v_{DS} = V_{DD} - i_D R_D = 10\text{V} - (3.125\text{mA})(2\text{k}\Omega) = 3.75\text{V}$$

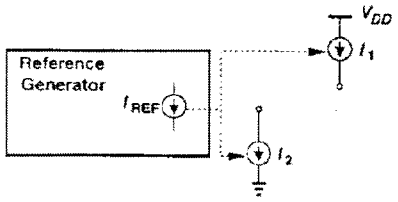
$$v_{GS} - V_T = 4\text{ V} - 1.5\text{ V} = 2.5\text{ V}$$

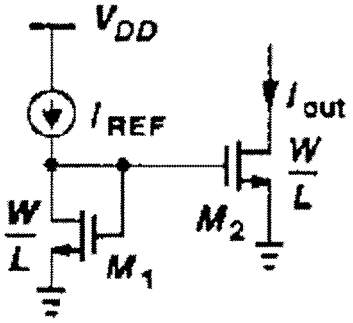
$v_{DS} > v_{GS} - V_T$ → saturation confirmed.

2

3+4+4+4

35





$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2,$$

Case 3: $V_D = 0$ V.

$V_{SG} = 5 - 0 = 5\text{ V} > |V_t| \Rightarrow$ not cutoff! $\quad V_{DG} = 0 - 0 = 0\text{ V} \le |V_t| \Rightarrow$ in Saturation!

$$I_D = \frac{k_p'}{2} \times \frac{W}{L}(V_{SG} - |V_t|)^2(1 + |\lambda| V_{SD})$$

$$I_D = \frac{80\times10^{-6}}{2}(5 - |-1.5|)^2\left[1 + |-0.02| \times (5 - 0)\right] \quad \rightarrow I_D = 40\times10^{-6} \times 3.5^2 \times 1.1 = 539\ \mu\text{A}$$