Roll No.						



PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations - MAY 2025

School: SOCSE	Program: B. Tech-CSE				
Course Code: CSE2009	Course Name: Computer Organization and Architecture				
Semester: IV	Max Marks: 100	Weightage: 50%			

CO - Levels	CO1	CO2	CO3	CO4	CO5
Marks	26	26	24	24	-

Instructions:

- (i) Read all questions carefully and answer accordingly.
- (ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks.

10Q x 2M=20M

1.	List the functional units of computer system.	2 Marks	L1	CO1
2.	Distinguish between CISC and RISC Processor.	2 Marks	L2	CO1
3.	Summarize the type of ROM used in computer system.	2 Marks	L2	CO2
4.	Outline the processor execution time equation of a computer system.	2 Marks	L1	CO1
5.	Distinguish between PUSH and POP instruction with examples.	2 Marks	L2	CO2
6.	Distinguish between MAR and MDR in Computer Architecture.	2 Marks	L2	CO2
7.	Compute the recoded form of the sequence (10110111) ₂ using the Booth's Algorithm Recoding Table.	2 Marks	L2	CO3
8.	Outline the flowchart of Programmed I/O Communication Technique.	2 Marks	L1	CO3
9.	Outline the control sequence for the instruction ADD R1, R2, R3 in Single Bus architecture.	2 Marks	L1	CO4
10.	List the tasks involved in pipelining concepts of computer system.	2 Marks	L1	CO4

Part B

Answer the Questions.

11. a. Distinguish between the big endian assignment and little 4 Marks L2 CO1

Total Marks 80M

	-	endian assignment with suitable example.			331
	b.	Explain the types of instructions based on addresses with suitable examples.	6 Marks	L2	CO1
	C.	Compute the overflow values for the 5-bit signed number addition of the following i. $(-12) + (-10)$ ii. $(-9) - (-13)$ iii. $(-11) + (-8)$ iv. $(-9) - (-8)$ v. $(+14) + (-7)$	10 Marks	L2	CO1
		0r			
12.	a.	Explain the communication between the Processor and Memory with block diagram.	4 Marks	L2	CO1
	b.	Describe the purpose of bus structure in Computer System with necessary blocks.	6 Marks	L2	CO1
	C.	Summarize the architecture of Single Bus architecture and Multiple Bus architecture with block diagram.	10 Marks	L2	CO4
13.	a.	Explain Memory Hierarchy in computers with a neat diagram.	4 Marks	L2	CO2
	b.	i. ADD (R3)+, R4 ii. STORE 100(R3,R2),(R4) iii. MOV #4004, R2 iv. LOAD 14(R2),R7 v. SUB -(R1),R2 vi. STORE 50(R4),R1	6 Marks	L2	CO2
	c.	Consider a cache consisting of 256 blocks of 16 words each, for a total of 4096 words and assume main memory is addressable by 16 bit address and it consists of 4K blocks. Calculate the mapping formats for the different mapping techniques.	10 Marks	L3	CO2
		Or			
14.	a.	Explain about Cache memory and its usage in Computer organization.	4 Marks	L2	CO2
	b.	Describe the memory read/write operation of the 16 X 8 Internal Memory chip.	6 Marks	L2	CO2
	c.	Illustrate the various addressing modes of computer instructions with examples.	10 Marks	L3	CO2
15.	a.	Covert the following values to Single Precision Floating Point. i) -0.011561 ii) +0.000789	4 Marks	L2	CO3
	b.	Make use of Sign Extension algorithm to solve the multiplication of (+31) and (-28).	6 Marks	L3	CO3

		Domonstrate the 4 hit adder singuit to reduce the later or in the	10 Marilya	1.2	CO2
	C.	Demonstrate the 4 bit adder circuit to reduce the latency in the	10 Marks	L3	CO3
		propagation of the Carry signal with necessary diagrams.			
		0r			
16 .	a.	Convert the following values to Single Precision Floating Point	4 Marks	L2	CO3
		i) -0.001786			
		ii) +0.23546			
	b.	Make use of Booth's algorithm to solve the multiplication of	6 Marks	L3	CO3
		(+22) and (-19)			
	c.	Utilize the Restoration Method to solve the division of 15 by 9.	10 Marks	L3	CO3
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17.	a.	Distinguish between Memory mapped IO and I/O mapped I/O.	4 Marks	L2	CO4
	b.	Describe the importance of Direct Memory Access controller	6 Marks	L2	CO4
		with architecture			
	c.	Identify the control sequence for the instruction of ADD	10 Marks	L1	CO4
		(R2), R1 for the Single Bus Architecture with diagram.			
	- II	Or		I.	I.
18.	a.	Explain about the Interrupt based I/O Communication	4 Marks	L2	CO4
	b.	Identify the control sequence for the instruction of ADD	6 Marks	L1	CO4
		R3,R4,R5 for the Multiple Bus Architecture with diagram			
	C.	Describe the types of hazards in pipelining with necessary	10 Marks	L2	CO4
		diagram.			