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**PRESIDENCY UNIVERSITY**

**Bengaluru**

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| **End - Term Examinations – MAY 2025** |
| **Date:** 22-05-2025 **Time:** 01:00 pm – 04:00 pm |

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| **School:** SOIS | **Program:** BCA/BCADS/BCAAIML | |
| **Course Code:** CSA2002 | **Course Name:** Computer Organization | |
| **Semester**: II | **Max Marks**: 100 | **Weightage**: 50% |

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| **CO - Levels** | **CO1** | **CO2** | **CO3** | **CO4** | **CO5** |
| **Marks** | **24** | **26** | **26** | **24** | **NA** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Do not write anything on the question paper other than roll number.*

**Part A**

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| **Answer ALL the Questions. Each question carries 2marks. 10Q x 2M=20M** | | | | |
| **1.** | Give an example of a three-address instruction. | **2 Marks** | **L1** | **CO1** |
| **2.** | If a computer has a 32-bit address bus, what is the maximum memory it can address? | **2 Marks** | **L1** | **CO1** |
| **3.** | List two common memory operations. | **2 Marks** | **L1** | **CO2** |
| **4.** | List two types of ROM. | **2 Marks** | **L1** | **CO2** |
| **5.** | Define cache memory. | **2 Marks** | **L1** | **CO2** |
| **6.** | List four examples of peripheral devices. | **2 Marks** | **L1** | **CO3** |
| **7.** | What is the main advantage of a carry look-ahead adder? | **2 Marks** | **L1** | **CO3** |
| **8.** | What is DMA? | **2 Marks** | **L1** | **CO3** |
| **9.** | What is a single bus organization in a computer system? | **2 Marks** | **L1** | **CO4** |
| **10.** | How is a word fetched from memory? | **2 Marks** | **L1** | **CO4** |

**Part B**

**Answer the Questions. Total Marks 80M**

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| 11. | a. | Show the connection between the processor and memory, including the use of cache. | 8 Marks | L2 | CO1 |
|  | **b.** | Solve following operations on 5-bit signed numbers using 2’s complement representation system. Also predict whether overflow has occurred or not.   1. -9 -7 2. +7 –(-8) 3. -10 – (- 13)   d) (-10) +(-13) | **8 Marks** | **L3** | **CO1** |
|  | **c.** | A Program has 100 machine instructions in a straight line code and 100 instructions in a loop which gets executed for 49 times. The average number of basic steps needed to execute one machine instruction is 2 cycles and the processor is controlled by a clock of 2GHz. Calculate the time required for the program execution. | **4 marks** | **L3** | **CO1** |
| Or | | | | | |
| 12. | **a.** | Describe the functional units of a computer with a detailed block diagram. | **8 Marks** | **L2** | **CO1** |
|  | **b.** | Evaluate E=(A+B)\*(C+D) using one address , Two-Address and Three-address instruction format | **8 Marks** | **L3** | **CO1** |
|  | **c.** | A program contains 1000 instructions. Out of that 25% instructions requires 4 clock cycles, 40% instructions requires 5 clock cycles and remaining requires 3 clock cycles for execution. Calculate the total time required to execute the program running in a 1 GHz machine. | **4 marks** | **L3** | **CO1** |

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| 13. | a. | Consider a cache consisting of 256 blocks of 16 words each, for a total of 4096 words and assume main memory is addressable by 16 bit address and it consists of 4K blocks. Calculate the number of bits in each of Tag, block/set and word fields for direct mapping technique. | 8 Marks | L3 | CO2 |
|  | **b.** | Explain the various addressing modes with suitable examples. | **8 Marks** | **L2** | **CO2** |
|  | **c.** | Describe the advantages and disadvantages of using Read Only Memory (ROM). | **4 Marks** | **L2** | **CO2** |
| Or | | | | | |
| 14. | **a.** | Consider a cache consisting of 128 blocks of 4 words each and main memory consisting of 4096 blocks. i) How many bits for memory address? ii) How many bits for representing tag, block and word fields? For Associative mapping techniques. | **8 Marks** | **L3** | **CO2** |
|  | **b.** | Explain the organization of cache memory and discuss the different cache mapping techniques (direct, associative, and set-associative). | **8 Marks** | **L2** | **CO2** |
|  | **c.** | Explain DMA operational modes. | **4 Marks** | **L2** | **CO2** |

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| 15. | a. | Describe an 4-bit carry look ahead adder and explain its working with an example. | 8 Marks | L2 | CO3 |
|  | **b.** | Calculate product of two numbers using the booths algorithm for given inputs 15 and 9. | **8 Marks** | **L3** | **CO3** |
|  | **c.** | Describe the logic diagram of a 4-bit full adder unit. | **4 Marks** | **L2** | **CO3** |
| Or | | | | | |
| 16. | **a.** | Calculate integer division using the restoring division algorithm for given inputs, 10 divided by 3. | **8 Marks** | **L3** | **CO3** |
|  | **b.** | With a suitable diagram, explain the working of a memory-mapped I/O system and I/O mapped I/O. | **8 Marks** | **L2** | **CO3** |
|  | **c.** | Calculate the product of (-13) and (+11) bit using 5 bit sign extension. | **4 Marks** | **L2** | **CO3** |

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| 17. | a. | Explain the steps involved in executing a complete instruction, including fetching, decoding, and execution. | 8 Marks | L2 | CO4 |
|  | **b.** | Illustrate the control sequence for storing a word in memory with a diagram for the instruction MOV R2,(R1). | **8 Marks** | **L3** | **CO4** |
|  | **c.** | How are arithmetic or logic operations performed in a processing unit? | **4 Marks** | **L2** | **CO4** |
| Or | | | | | |
| 18. | **a.** | Explain the 3 operations involved in executing the instruction. | **8 Marks** | **L2** | **CO4** |
|  | **b.** | Describe the role of multiple bus organization in improving processor performance. | **8 Marks** | **L2** | **CO4** |
|  | **c.** | Describe the control sequence involved in fetching a word from memory, MOV (R1),R2. | **4 Marks** | **L2** | **CO4** |

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