| Roll No. | | | | | | | | | | | | |
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# PRESIDENCY UNIVERSITY

## BENGALURU

**End - Term Examinations – MAY/ JUNE 2025**

**Date:** 03-06-2025 **Time:** 01:00 pm – 04:00 pm

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|---|---|---|
| **School :** SOCSE/SOE | **Program :** B .Tech-Physics Cycle | |
| **Course Code :** ECE2007 | **Course Name :** DIGITAL DESIGN | |
| **Semester :** II | **Max Marks**: 100 | **Weightage**: 50% |

| **CO - Levels** | **CO1** | **CO2** | **CO3** | **CO4** | **CO5** |
|---|---|---|---|---|---|
| **Marks** | **10** | **20** | **20** | **25** | **25** |

**Instructions:**

*(i) Read all questions carefully and answer accordingly.*

*(ii) Do not write anything on the question paper other than roll number.*

## Part A

**Answer ALL the Questions. Each question carries 2marks.** **10Q x 2M=20M**

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|---|---|---|---|---|
| **1.** | In the given Truth Table X, Y, Z are input literals(variables) and F is output literal. In terms of input literals, Express the Canonical Product of Sum (Canonical PoS) Equation for the output F: | **2 Marks** | **L2** | **CO2** |
| **2.** | To Implement a four variable Boolean function, how many number of 8X1 MUX(Multiplexers) needed? | **2 Marks** | **L2** | **CO2** |
| **3.** | Write the name of the logic circuit which is used to select one data from several input data with the help of selection lines : | **2 Marks** | **L2** | **CO2** |
| **4.** | In 8 into 3 line Priority Encoder circuit, input data line D3, D2 & D0 are high means what is the encoded binary value of Encoder? | **2 Marks** | **L2** | **CO2** |
| **5.** | Draw the circuit of 1x2 DMUX using basic gates: | **2 Marks** | **L2** | **CO2** |

| X | Y | Z | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

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|---|---|---|---|---|
| **6.** | Write the Characteristics table(Functional Table) of D flip-flop: | **2 Marks** | **L2** | **CO3** |
| **7.** | Write the Characteristics Equation of D Flip Flop: | **2 Marks** | **L2** | **CO3** |
| **8.** | How many JK flip-flops are required to design an N-bit synchronous counter? | **2 Marks** | **L2** | **CO3** |
| **9.** | Mention one key difference between a latch and a flip-flop: | **2 Marks** | **L2** | **CO3** |
| **10.** | Which flip-flop encounters a forbidden state, and under what input combination does this occur? | **2 Marks** | **L2** | **CO3** |

**Part B**

**Answer the Questions.** **Total Marks 80M**

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|---|---|---|---|---|---|
| **11.** | **a.** | Find the minimum Product of Sum (PoS) expression using Karnaugh Map for the function:**(A,B,C,D)=Σm(0,1,4,6,8,9,14,15).** Also construct corresponding logic circuit using only NOR gates: | **10 Marks** | **L3** | **CO1** |
| | | **Or** | | | |
| **12.** | **a.** | Determine the minimum SoP for the given Boolean function using K Map **F(A,B,C,D)=Σm(0,1,4,6,9, 14,15)+ DC(2,8)**.Also draw the logic circuit using NAND gate only: | **10 Marks** | **L3** | **CO1** |
| **13.** | **a.**<br>**b.** | Draw the ExNOR gate logic circuit using minimum NOR gate:<br>Using two Half Adders and an AND gate, how can a Full Adder circuit be designed? Provide a step-by-step derivation of the logic circuit from its truth table. | **2 Marks**<br>**8 Marks** | **L3**<br>**L3** | **CO2**<br>**CO2** |
| | | **Or** | | | |
| **14.** | **a.**<br>**b.** | Draw the ExOR gate logic circuit using minimum NOR gate:<br>Using two Half Subtractor and an AND gate, how can a Full Subtractor circuit be designed? Provide a step-by-step derivation of the logic circuit from its truth table: | **2 Marks**<br>**8 Marks** | **L3**<br>**L3** | **CO2**<br>**CO2** |
| **15.** | **a.** | Using 4x1 MUX, Implement the given Boolean function Y:<br>**Y=Σm( 1,2,4,11,12, 13,14,15)** | **10 Marks** | **L3** | **CO4** |
| | | **Or** | | | |
| **16.** | **a.**<br>**b.** | Design Full Adder using 3 into 8-line Decoder:<br>Implement 8x1 MUX using possible lower order MUX(If needed use Gates also): | **5 Marks**<br>**5 Marks** | **L3**<br>**L3** | **CO4**<br>**CO4** |
| **17.** | **a.** | Design a combinational logic circuit with valid output bit, Which is used for Priority based 4 into 2 line Encoder: | **15 Marks** | **L3** | **CO4** |
| | | **Or** | | | |
| **18.** | **a.** | Design a TWO BIT Magnitude Comparator Circuit: | **15 Marks** | **L3** | **CO4** |
| **19.** | **a.**<br>**b.** | Draw the block diagram of PIPO shift registers using D Flip-Flop:<br>Draw the logic circuit of JK Flip-Flop with clock signal and derive the following characteristics:<br>i) Characteristic Table<br>ii) Characteristic Equation (Next State Equation)<br>iii) Excitation Table | **5 Marks**<br>**10 Marks** | **L3**<br>**L3** | **CO5**<br>**CO3** |
| | | **Or** | | | |
| **20.** | **a.** | Draw the block diagram of SIPO shift registers using D Flip-Flop: | **5 Marks** | **L3** | **CO5** |

| | | | | | |
|---|---|---|---|---|---|
| | **b.** | Illustrate the logic circuit of an SR latch with an Enable input and derive its following characteristics:<br>i) Characteristic Table<br>ii) Characteristic Equation (Next State Equation)<br>iii) Excitation Table | **10 Marks** | **L3** | **CO3** |

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|---|---|---|---|---|---|
| **21.** | **a.** | Design a 3-bit synchronous counter using JK flip-flops, incorporating a state diagram and table to illustrate counting from 7 to 0 (DOWN COUNTER): | **20 Marks** | **L3** | **CO5** |
| | | **Or** | | | |
| **22.** | **a.** | Design a 4-bit synchronous counter using D flip-flops, incorporating a state diagram and table to illustrate counting from 0 to 15 (UP COUNTER): | **20 Marks** | **L3** | **CO5** |