PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – MAY 2025

Date: 29-05-2025   **Time:** 09:30 am – 12:30 pm

School: SOE	**Program:** B. Tech
Course Code: ECE3014	**Course Name**: Microcontroller Applications
Semester: VI	**Max Marks**: 100 **Weightage**: 50%

CO - Levels	CO1	CO2	CO3	CO4	CO5
Marks	24	24	26	26	

Instructions:

(i) *Read all questions carefully and answer accordingly.*

(ii) *Do not write anything on the question paper other than roll number.*

Part A

Answer ALL the Questions. Each question carries 2marks.   **10Q x 2M=20M**

1.	State the word size for arithmetic and logical operations, and the internal bus width of 32 bit microcontroller	2 Marks	L1	CO1
2.	In 8051 microcontroller state the functions of the ALE, PSEN pins	2 Marks	L1	CO1
3.	State the operations of the XRL and ORL instructions in 8051	2 Marks	L1	CO2
4.	Find the contents of register A on execution of the following code SET C MOV A, #9BH RRC A	2 Marks	L1	CO2
5.	State the functions of each bit of the SCON register	2 Marks	L1	CO3
6.	Compute the initial value for timer in mode 1 to obtain the time delay of 12uS, given the crystal frequency is 11.0592 MHz	2 Marks	L1	CO3
7.	State the difference between half duplex and full duplex serial communication	2 Marks	L1	CO3
8.	What are some common applications of ARM microcontrollers in the real world?	2 Marks	L1	CO4

9.	State the three stages of pipline in instruction execution	2 Marks	L1	CO4
10.	What is the difference between ARM and Thumb instructions?	2 Marks	L1	CO4

Part B

Answer the Questions.   **Total Marks 80M**

11.	a.	Compare Von Neumann architecture and Harvard architecture	10 Marks	L2	CO1
	b.	Design a μController system using 8051. Interface the external RAM of size 8k x 8. Compute the address decoding map and interface the memory such that starting address for RAM is 7000H	10 Marks	L2	CO1
		Or			
12.	a.	Explain with neat diagram the external data memory (RAM) interfacing and the timing diagram of WRITE cycle.	10 Marks	L2	CO1

	b.	Examining the stack, show the contents of the register and SP after execution of the following instructions.
		
		MOV SP, #49H
		MOV R3, #84H
		MOV R5, #0BAH
		MOV R6, #70H
		PUSH 5
		PUSH 6
		POP 2
		PUSH 3
		POP 1
		POP 3
			10 Marks	L2	CO1

13.	a.	Determine the contents of Registers, Memory and the status Flags after execution of each instruction sequentially.	10 Marks	L3	CO2

Instructions	Binary value	Hex Value	Status Flags C, AC, P		
MOV A, #9AH	A=	A=	C=	AC=	P=
MOV R2, #0A2H	R2=	R1=	C=	AC=	P=
ADD A, R2	A=	A=	C=	AC=	P=
RLC A	A=	A=	C=	AC=	P=
SWAP A	A=	A=	C=	AC=	P=
DEC R2	R2=	R1=	C=	AC=	P=
ANL A, R2	A=	A=	C=	AC=	P=

		RR A	A=	A=	C= AC= P=		
		CPL A	A=	A=	C= AC= P=		
		XRL A, A	A=	A=	C= AC= P=		

	b.	Write an Assembly language program to perform subtraction of seven bytes stored at memory location 42H onwards with bytes stored at location 48H onwards. Store the result at memory location 58H onwards.	**10 Marks**	L3	CO2
		**Or**			
14.	a.	Write the truth table for the following SOP Boolean expression and write an ALP to realize the expression. P = XY'Z + XY'Z' + X'Y'Z' + X'YZ	**10 Marks**	L3	CO2
	b.	Explain with examples the following instructions (a) JNB, (b) ORL, (c) SWAP, (d) DJNZ, (e) DA A	**10 Marks**	L3	CO2

15.	a.	8051 consist of Serial communication. Explain the registers associated with Serial communication.	**10 Marks**	L3	CO3
	b.	Generate a rectangular wave of 1.25kHz, with 45% duty cycle in P2.3. Assume crystal frequency as 11.0592MHz, use Timer 1 in Mode 1 operation. Show the delay calculation.	**10 Marks**	L3	CO3
		Or			
16.	a.	Write a Assembly language program for 8051 to transfer the message "FAN" serially at 9600 baud rate continuously. Assume crystal frequency at 11.0592MHz. Show the timing calculations	**10 Marks**	L3	CO3
	b.	8051 consist of two timers. Explain the registers associated with timer to activate and configure.	**10 Marks**	L3	CO3

17.	a.	Describe with neat diagram the Banked registers and the Processor modes of ARM processor	**10 Marks**	L3	CO4
	b.	The ARM uses the Current Program Status Register (CPSR) to monitor and control internal operations. Describe with diagram the CPSR in ARM processor	**10 Marks**	L3	CO4
		Or			
18.	a.	Explain with diagram the ARM core data flow model	**10 Marks**	L3	CO4
	b.	A major design rule in the RISC design philosophy is Pipeline. Explain with appropriate diagram the pipeline mechanism in RISC processor	**10 Marks**	L3	CO4