Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – MAY/ JUNE 2025

Date: 05-06-2025 **Time:** 09:30 am – 12:30 pm

School: SOE	**Program:** B. Tech (ECE)	
Course Code: ECE3046	**Course Name**: Low Power VLSI Design	
Semester: VI	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	**CO1**	**CO2**	**CO3**	**CO4**
Marks	**12**	**16**	**36**	**36**

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1.	List the sources of glitch power dissipation.	**2 Marks**	**L1**	**CO1**
2.	Define subthreshold leakage current.	**2 Marks**	**L1**	**CO1**
3.	Illustrate Event-driven logic simulation.	**2 Marks**	**L1**	**CO2**
4.	List out the advantages of GLS.	**2 Marks**	**L1**	**CO2**
5.	Differentiate best case and worst case in gate sizing.	**2 Marks**	**L1**	**CO3**
6.	Illustrate equivalent pin ordering.	**2 Marks**	**L1**	**CO3**
7.	Define signal gating.	**2 Marks**	**L1**	**CO3**
8.	Illustrate self-gating flip flop.	**2 Marks**	**L1**	**CO4**
9.	What is the difference between NAP and Doze mode?	**2 Marks**	**L1**	**CO4**
10.	Define tolerable skew.	**2 Marks**	**L1**	**CO4**

Part B

Answer the Questions. **4Q x 20M=80M**

11.	**a.**	(i) The Monte Carlo simulation is a mathematical technique that predicts possible outcomes of an uncertain event.	**20 Marks**	**L2**	**CO1& 2**

		Computer programs use this method to analyze past data and predict a range of future outcomes based on a choice of action. Describe Monte Carlo simulation technique. (ii) VTCMOS is one of the methods to reduce leakage power. Explain VTCMOS.			
		Or			
12.	**a.**	(i) The leakage power dissipation is one of the main sources of power dissipation. Describe reverse diode leakage current. (ii) The designer can apply low-power techniques at the architecture level. Explain advantages of pipelining over parallel processing.	**20 Marks**	**L2**	**CO1& 2**

13.	**a.**	(i) The power dissipation is reduced using transistor sizing method. Realize the Boolean function f=(A(BC+D)+DE)'. Find an equivalent CMOS inverter circuit for simultaneous switching of all input. Given (W/L)P=15 for all PMOS and (W/L)N=10 for all NMOS.	**20 Marks**	**L3**	**CO3**
		Or			
14.	**a.**	The logic encoding has a great impact on reduction of switching activity in the circuit. Illustrate logical encoding and prove that gray code is an efficient coding than binary coding for low power counter circuit design.	**20 Marks**	**L3**	**CO3**

15.	**a.**	The low-power technique is implemented at the circuit level. Describe (i) Network restructuring and reorganization (ii) Local Restructuring.	**20 Marks**	**L3**	**CO4**
		Or			
16.	**a.**	(i)Precomputation logic has a great impact on reduction of switching activity in the circuit. Describe precomputation logic. (ii) The buffers are inserted in the clock tree. Illustrate need for buffer in clock tree and describe different types of buffers in clock tree.	**20 Marks**	**L3**	**CO4**

17.	**a.**	(i) Performance management is an important issue in architecture-level management. Explain power and performance management at architectural level. (ii) The full-swing clock increases the power dissipation of the circuit. Hence, the reduced swing clock circuit is designed to reduce power dissipation. Describe switching activity reduction method.	**20 Marks**	**L3**	**CO3 &4**
		Or			
18.	**a.**	Adaptive design is an effective method of reducing power dissipation of the circuit. (i) Describe adaptive performance management by voltage control . (ii) Explain oscillator circuit for clock generation.	**20 Marks**	**L3**	**CO3 &4**