Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – MAY 2025

Date: 28-05-2025 **Time:** 01:00 pm – 04:00 pm

School: SOE	**Program:** B. Tech VLSI	
Course Code: ECE3164	**Course Name:** Introduction to Fabrication Technology	
Semester: IV	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	CO1	CO2	CO3	CO4	CO5
Marks	24	22	22	32	

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1.	Mention the equations for the Linear and Parabolic rate constants that apply in the Deal-Grove model of oxidation.	**2 Marks**	**L1**	**CO2**
2.	List out the scenarios/applications for which we use wet oxidation.	**2 Marks**	**L3**	**CO2**
3.	Discuss in brief the impact of the presence of Grain Boundaries in the Silicon crystal.	**2 Marks**	**L3**	**CO1**
4.	A clean room is required for the fabrication processes to be carried out. Mention the purposes for which a clean room is used.	**2 Marks**	**L2**	**CO1**
5.	List out the popular Lithography techniques used in the semiconductor industry.	**2 Marks**	**L1**	**CO2**
6.	Briefly explain the parameter 'Resolution' used in the Lithography of semiconductor devices.	**2 Marks**	**L2**	**CO2**
7.	Discuss the significance of Annealing in the diffusion process.	**2 Marks**	**L2**	**CO4**
8.	Explain in brief with an example, the precursor gases in the diffusion process.	**2 Marks**	**L2**	**CO4**

9.	Briefly explain the 'Aspect Ratio' that is used as a parameter in the etching process.	**2 Marks**	**L2**	**CO3**
10.	With the necessary formula, explain Selectivity in the etching process in short.	**2 Marks**	**L2**	**CO2**

Part B

Answer the Questions. **Total Marks 80M**

11.	**a.**	Give a brief explanation of Front End of the Line (FEOL) and Back End of the Line (FEOL) cleaning in relation to semiconductor fabrication processes.	4 Marks	**L2**	**CO1**
	b.	Single-crystalline silicon ingots are used to cut wafers, which are then utilized to fabricate semiconductor devices. Give a description of the electrical, optical, mechanical, and purity attributes of single-crystalline silicon in this context.	8 Marks	**L3**	**CO1**
	c.	A critical consideration in the fabrication of semiconductor devices on silicon wafers is yield. Describe "Yield" using the required formula. Provide a brief description of the factors influencing yield and the consequences of low yield.	8 Marks	**L4**	**CO1**
		Or			
12.	**a.**	Irregularities in the regular arrangement of atoms within a crystalline solid are referred to as crystal defects, and they affect the material's physical characteristics. List out defect types that can be present in the crystal and briefly explain the Line Defects and their types.	8 Marks	**L2**	**CO1**
	b.	Silicon wafers may suffer from contaminants introduced during fabrication processes. A clean room is therefore necessary. List the different clean room design types and differentiate between "ballroom" and "tunnel" design types.	8 Marks	**L4**	**CO1**
	c.	In order to reduce the presence and impact of contaminants, clean rooms are used in semiconductor fabrication processes. Give a brief explanation of the "HEPA" filters that are utilized in the clean room design.	4 Marks	**L2**	**CO1**

13.	**a.**	Thin Film Deposition is the technology of applying a very thin film of material – between a few nanometers to about 100 micrometers, or the thickness of a few atoms – onto a "substrate" surface to be coated. With the help of a neat and labelled diagram, explain the working principle of Sputtering i.e. another thin film deposition technique.	8 Marks	**L2**	**CO4**
	b.	Silicon wafer oxidation is a process where an oxide layer, typically silicon dioxide (SiO_2), is grown on the surface of a silicon wafer. Under this pretext, explain the four critical advantages of High-Pressure Oxidation over Thermal Oxidation of Silicon wafer.	8 Marks	**L2**	**CO2**

	c.	In the context of thermal oxidation of Silicon wafer, explain in brief with the necessary equations, the effect of pressure on the Parabolic Rate Constant, in the Deal-Grove Model.	4 Marks	**L3**	**CO2**
		Or			
14.	**a.**	In the context of thermal oxidation of Silicon wafer, explain, why is it important to control temperature and ambient gas composition during the oxidation process?	4 Marks	**L3**	**CO2**
	b.	The Deal-Grove model is a mathematical model that describes the thermal oxidation of silicon wafer. In this context, with the help of necessary graphs, explain the effect of temperature on the parabolic and linear rate constants for both dry and wet oxidation.	8 Marks	**L4**	**CO2**
	c.	Packaging refers to the process of protecting and connecting semiconductor chips for reliable performance and ease of use in electronic devices. Mention and briefly explain the common types of packaging techniques in the semiconductor industry.	8 Marks	**L2**	**CO4**

15.	**a.**	Photolithography is a type of lithographic method performed after preparing the wafer and growing the oxide layer. In semiconductor device fabrication, describe in detail the various steps involved in the photolithography process.	10 Marks	**L2**	**CO3**
	b.	One of the key parameters in different lithographic methods is resolution. Discuss the factors that influence the resolution of a lithographic technique.	5 Marks	**L2**	**CO3**
	c.	Wet Etching and Dry Etching are the two main types of Etching techniques. Differentiate between the two considering important etching parameters.	5 Marks	**L4**	**CO3**
		Or			
16.	**a.**	Discuss in brief the Proximity Effects that occur in Lithographic techniques like Electron Beam Lithography (EBL) and Ion Beam Lithography.	4 Marks	**L3**	**CO3**
	b.	After Lithography, Etching is carried out to remove the selective regions of the substrate. In this regard, discuss in detail, the four main etching parameters that are involved in the wet etching process.	8 Marks	**L2**	**CO3**
	c.	Photolithography and X-ray Lithography are the two prominent Lithographic techniques. Differentiate between these two techniques considering important Lithography parameters.	8 Marks	**L4**	**CO3**

17.	**a.**	The diffusion process is carried out after Lithography and Etching for the introduction of dopants into the substrate. In this regard, explain the Fick's First and Second Law of Diffusion with necessary equations and graphs.	10 Marks	**L2**	**CO4**
	b.	In the context of diffusion, explain the Dopant Precursors. Citing relevant examples mention the physical states in which the Precursors are used in the diffusion process.	06 Marks	**L3**	**CO4**

	c.	Briefly explain the purpose of using an inert gas like N_2 (Nitrogen) in the Diffusion furnace.	04 Marks	**L2**	**CO4**
		Or			
18.	**a.**	The introduction of dopants or impurities into the substrate is done through the diffusion process. Briefly explain the Lateral Diffusion of the dopants with a suitable diagram.	04 Marks	**L2**	**CO4**
	b.	Thermal Diffusion and Ion Implantation are the two main techniques used for introducing the dopants into the substrate. Considering key diffusion parameters differentiate between these two techniques.	06 Marks	**L4**	**CO4**
	c.	Plasma-Enhanced Chemical Vapor Deposition (PECVD) is a widely used thin-film deposition technique in semiconductor manufacturing and other applications. With a neat and labelled diagram, explain the working mechanism and the role of Plasma in PECVD.	10 Marks	**L2**	**CO4**