Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – MAY 2025

Date: 29-05-2025 **Time:** 09:30 am – 12:30 pm

School: SOE	**Program:** B. Tech (EEE)	
Course Code: EEE3013	**Course Name:** VLSI Design	
Semester: VI	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	CO1	CO2	CO3	CO4
Marks	26	24	26	24

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. 10Q x 2M=20M

1.	List two advantages of assembling electronic components using IC technology.	**2 Marks**	**L1**	**CO1**
2.	List two disadvantages of assembling electronic components using discrete components.	**2 Marks**	**L1**	**CO1**
3.	Write the Verilog code for a 2-input AND gate using data flow modeling.	**2 Marks**	**L1**	**CO1**
4.	If an n-MOS enhancement MOSFET has V_{TH} =0.5 V, what should be the minimum V_{GS} to turn it ON?	**2 Marks**	**L1**	**CO2**
5.	What is the difference between enhancement-mode and depletion-mode MOSFETs?	**2 Marks**	**L1**	**CO2**
6.	What are the advantages of Static CMOS design?	**2 Marks**	**L1**	**CO3**
7.	Mention three differences between Static CMOS design and Dynamic CMOS design.	**2 Marks**	**L1**	**CO3**
8.	What do you mean by Signal Integrity Issues in Dynamic CMOS Logic?	**2 Marks**	**L1**	**CO3**
9.	What is Parallel Adder?	**2 Marks**	**L1**	**CO4**
10.	What is Booth Multiplier?	**2 Marks**	**L1**	**CO4**

Part B

Answer the Questions. Total Marks 80M

11.	**a.**	VLSI design methodology plays a crucial role in developing complex integrated circuits by following a systematic approach.	**10 Marks**	**L1**	**CO1**

		Explain the VLSI design methodology in detail, illustrate it with a pictorial representation, and describe the different design domains involved in the process.			
	b.	A 4:1 Multiplexer (MUX) is a combinational circuit that selects one of four input signals and forwards it to the output based on the values of two selection lines (S1, S0). Multiplexers are widely used in digital circuits for data selection, signal routing, and logic design. How can a 4:1 Multiplexer be implemented using Behavioral Modeling in Verilog? Write and explain the Verilog code for designing a 4:1 MUX.	**10 Marks**	**L2**	**CO1**
		Or			
12.	**a.**	In IC design, the principles of Hierarchy, Modularity, Regularity, and Locality help manage complexity and improve circuit efficiency. Regularity and Locality specifically contribute to optimizing design by ensuring structured repetition and minimizing interconnect delays. How do Regularity and Locality aid in reducing the complexity of VLSI design? Explain how regular structures simplify layout and how locality improves circuit performance.	**10 Marks**	**L1**	**CO1**
	b.	A Half Adder is a combinational circuit that performs the addition of two single-bit binary numbers. It has two inputs: A and B, and produces two outputs: Sum (S) and Carry (C_out). The Sum is given by $S=A \oplus B$, and the Carry is given by Cout=AB. The Half Adder is a fundamental building block in digital circuits, used in arithmetic operations and larger adder circuits. How can a Half Adder be implemented using Gate-Level Modeling in Verilog? Write and explain the Verilog code for designing a Half Adder using basic logic gates. Also, write a testbench to verify the functionality of the design for all possible input combinations.	**10 Marks**	**L2**	**CO1**
13.	**a.**	A p-channel MOSFET is a fundamental semiconductor device used in digital and analog circuits. It operates by modulating a p-type channel based on the applied gate-to-source voltage (V_{GS}). The current flows from the source to drain, and its conduction is controlled by the gate voltage relative to the source. How does the structure of a p-channel MOSFET influence its working principle? Explain the channel formation, current conduction mechanism detail.	**10 Marks**	**L3**	**CO2**
	b.	The given Boolean equation $Y = \overline{A.B}$ represents the NAND operation, which can be implemented using CMOS logic design. The circuit consists of pull-up (PMOS) and pull-down (NMOS) networks, ensuring proper logic functionality. A stick diagram is a simplified representation of the layout, showing the	**10 Marks**	**L3**	**CO2**

		interconnections of different layers (polysilicon, diffusion, and metal) in the fabrication process. How can the Boolean function Y = $\overline{A.B}$ be designed using CMOS logic? Draw the corresponding stick diagram and explain the role of pull-up and pull-down networks in circuit operation.			
		Or			
14.	**a.**	In an enhancement-mode MOSFET, the pinch-off condition occurs when the drain-to-source voltage (V_{DS}) increases to a point where the channel is completely depleted at the drain end. Beyond this point, further increases in V_{DS} do not significantly increase the drain current, leading to saturation. This condition is crucial in understanding the MOSFET's operation in the saturation region, where it functions as an amplifier. How does the pinch-off condition occur in an enhancement-mode MOSFET, and what is its significance in device operation? Illustrate and explain the formation of the pinch-off region and its impact on the MOSFET's characteristics.	**10 Marks**	**L3**	**CO2**
	b.	In a MOSFET operating in the saturation region, the drain current can be computed by substituting the given parameters (threshold voltage, oxide capacitance, electron mobility, W/L ratio, and applied voltages) into the appropriate equation. Understanding this calculation is essential for analyzing MOSFET performance in both analog and digital circuits. How is the drain current I_D is calculated in the saturation region of a MOSFET? The given parameters are: Threshold voltage, V_T= 0.8 V, Oxide capacitance per unit area, $C_{ox}= 3\times10^{-7}$ F/m^2, Electron mobility, μ_n= 0.06 m^2/V-sec. Width-to-length ratio, $\frac{W}{L}$=10, Gate-to-source voltage, V_{GS}= 2V, Drain-to-source voltage, V_{DS}= 3V.	**10 Marks**	**L3**	**CO2**
15.	**a.**	A half adder performs the addition of two single-bit binary numbers, generating a sum and a carry output. While traditionally implemented using basic logic gates like XOR and AND, the use of transmission gates allows for compact, full-swing CMOS logic implementation with better control over signal integrity and reduced delay. Transmission gate-based design avoids threshold voltage loss seen in pass-transistor logic, ensuring reliable arithmetic operations in low-power digital circuits. How can a half adder be designed using CMOS transmission gates, and what are the advantages of using this approach over conventional gate-based logic? Illustrate the circuit schematic using transmission gates, explain the logic-level operation for both sum and carry outputs, and analyze the functionality with respect to a complete truth table.	**10 Marks**	**L3**	**CO3**
	b.	In conventional CMOS static logic circuits, both NMOS and PMOS transistors are used in a complementary arrangement to	**10 Marks**	**L3**	**CO3**

		implement logic gates with low static power dissipation. When properly designed, one transistor network pulls the output high while the other pulls it low, ensuring minimal power is consumed in the steady state. This structure is foundational in digital VLSI design. Whereas Pseudo-CMOS circuits use only NMOS transistors along with a resistive or current-source-like PMOS load, mimicking the behavior of CMOS circuits but with fewer transistors. While simpler and sometimes faster in specific contexts, these circuits suffer from higher static power dissipation and degraded noise margins compared to conventional CMOS. They are often used in certain compact or low-cost logic designs. Design the conventional and Pseudo-CMOS circuits for the given expression: $Z = \overline{A + BC}$			
		Or			
16.	**a.**	In CMOS logic design, complex logic functions are implemented using complementary pull-up (PMOS) and pull-down (NMOS) networks to achieve full voltage swing, low static power, and robust noise margins. Given a specific logic function, the goal is to construct the corresponding CMOS circuit that realizes the function accurately. Furthermore, during simultaneous switching of all inputs, the equivalent inverter circuit helps in analyzing the effective sizing and performance. Transistor sizing, defined by the W/L ratio, plays a critical role in balancing the strength of PMOS and NMOS transistors to achieve optimal switching characteristics. How can a CMOS logic circuit be designed to realize the given function Z, and how can the equivalent inverter CMOS circuit be determined for simultaneous switching of all inputs? Assume W/L ratios of 15 for all PMOS transistors and 10 for all NMOS transistors. Illustrate the CMOS schematic for the logic function, explain the pull-up and pull-down network construction, and derive the equivalent inverter sizing for analyzing the overall switching behavior. $Z = \overline{F.(B + C).(D + E + A)}$	**20 Marks**	**L4**	**CO1**

17.	**a.**	In digital arithmetic operations, particularly in multiplication and multi-operand addition, the generation and propagation of carry bits can lead to significant delays. The Carry-Save Adder (CSA) is an efficient solution to this problem. Unlike traditional adders, a CSA does not immediately propagate the carry bits; instead, it saves them for later stages. This allows the adder to perform fast additions of three or more binary numbers by producing a partial sum and a carry vector, which can be added later using a conventional adder. CSAs are commonly used in	**20 Marks**	**L4**	**CO4**

		multipliers, MAC (multiply-accumulate) units, and digital signal processors (DSPs) for high-speed arithmetic operations. Explain the concept and working principle of a Carry-Save Adder (CSA). Design the logic diagram of a 4-bit Carry-Save Adder for adding three binary numbers. Write the Verilog code for the 4-bit Carry-Save Adder.			
		Or			
18.	**a.**	An Adder is a fundamental combinational circuit in digital electronics used to perform the arithmetic operation of addition. The simplest form of an adder is the Half Adder, which adds two single-bit binary numbers and produces a Sum and a Carry. However, Half Adders cannot handle carry inputs from previous stages. To overcome this limitation, the Full Adder was developed. A Full Adder adds three inputs: two significant bits and an input carry. It produces a Sum and a Carry-out, allowing for cascading multiple Full Adders to perform multi-bit binary additions. Adders are widely used in arithmetic and logic units (ALUs), processors, and digital signal processing applications. And hence describe a 4-bit parallel adder? Design the 4-bit parallel adder circuit. Also, write a Verilog program for the 4-bit parallel adder.	**20 Marks**	**L4**	**CO4**