ROLL NO.	
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PRESIDENCY UNIVERSITY, BENGALURU
SCHOOL OF ENGINEERING

Max Marks: 80 | Max Time: 120 Mins | Weightage: 40 %

ENDTERM FINAL EXAMINATION

I Semester AY 2017-18 Course: **ECE101 Elements of Electronics Engineering** 30 DECEM 2017

Instructions:

i. Write legibly
ii. Scientific and non-programmable calculators are permitted
iii. Assume standard values where required

Part A

[4 Q x 5 M= 20 Marks]

1. Perform the conversions (a) $(12)_{10}$ to $(\ )_2$ (b) $(12)_{10}$ to BCD
(c) $(B9A)_{16}$ to binary (d) $(101100)_2$ to octal (e) $(11001001)_2$ to hexadecimal

2. State *both* De Morgan's theorems, and prove *both* (by any method).

3. Perform the binary number subtraction $(1110)_2 - (11)_2$ in (a) one's complement (b) two's complement (c) convert the question to decimal and calculate the answer and verify the answer.

4. Name the three buses of Microprocessor 8085 and explain each with its purpose and its size.

Part B

[3 Q x 10 M= 30 Marks]

5. Draw the symbol, write equation and truth table for (a) AND (b) OR (c) XOR (d) NAND Gate

6. (a) Write the equation for the circuit given and simplify to simple SOP form using Boolean Laws

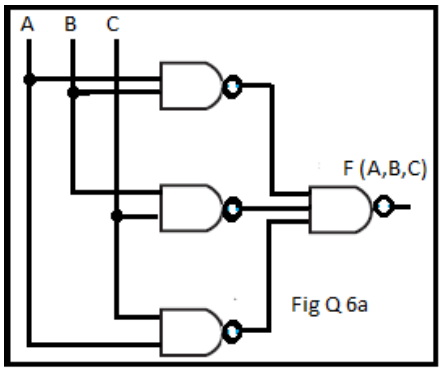

Fig Q 6a

(b) Simplify and implement f(p,q,r,s) = p'q'r's'+p'q'r's+p'q'rs'+p'q'rs+pqr's'+pqr's+pqrs'+pqrs

7. Why the NAND gate is called a Universal Gate? Draw the circuits to implement (a) NOT gate using NAND (b) AND gate using NAND (c) OR gate using NAND

Part C

[2 Q x 15 M= 30 Marks]

8. Draw and explain the detailed architecture of 8085 microprocessor with each section (ALU and its associate registers, Flags, Register Unit, Instruction Blocks and all other sections in full detail).

9. Simplify and implement using gates (a) F(P,Q,R) = Σ (3,5,6,7) (b) F(X,Y,Z) = XY+X'Z+YZ (c) $Y = AB + ABC + ABCD + ABCDE + ABD + ABE$

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Max Marks: 20 | Max Time: 60 Mins | Weightage: 20 %

TEST 2

I Semester 2017-2018 | Course: **ECE101 Elements of Electronics Engineering** | 25 Oct 2017

Instructions:

i. Write legibly.
ii. Make suitable assumptions for standard values where needed
iii. Scientific and non programmable calculators are permitted

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Part A

(3Q x 2 M= 06 Marks)

1. Draw the symbol and indicate E, B and C terminals for (a) NPN transistor (b) PNP Transistor.

2. In a certain transistor, collector current is 9mA and base current is 1mA. Determine the value of (a) Emitter current (b)α, β, γ

3. Explain why modulation is required in communication systems?

Part B

(2 Q x 3 M= 06 Marks)

4. Draw structure of N- Channel JFET and explain its working in detail, and the role of G, S, and D.

5. Explain with diagrams how a BJT can work as a switch / inverter

Part C

(2 Q x 4 M= 08 Marks)

6. Draw a Fixed bias circuit and explain how it works (for NPN transistor) and derive equations for I_B , I_C and $V_{CE.}$ If V_{CC} is 12V, R_B is 240 KΩ, R_C is 2.2 KΩ; and β is 50. Find I_B, I_C, V_{CE} at Q Point. Assume V_{BE} is 0.7V.

7. Draw the block diagram of communication systems and write a detailed short note on the same.

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Max Marks: 20 | Max Time: 60 Mins | Weightage: 20 %

TEST 1

I Semester 2017-2018 | Course: **ECE101 Elements of Electronics Engineering** | 20 SEPT 2017

Instructions:

i. Write legibly.
ii. Make suitable assumptions for standard values where needed
iii. Scientific and non programmable calculators are permitted

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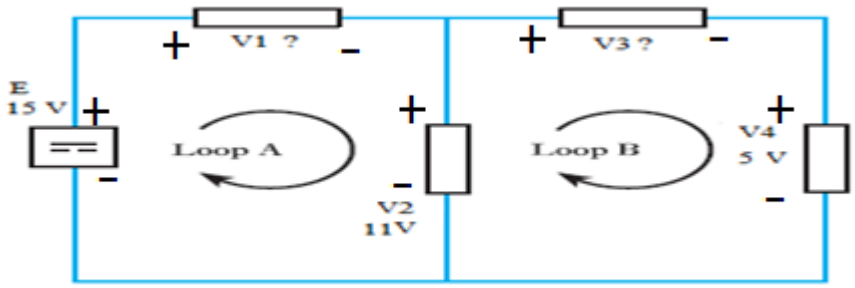
Part A

(3Q x 2 M= 06 Marks)

1. State Kirchhoff's Current Law (KCL) with relevant diagram
2. Write the equations (no derivations) for V_{DC}, V_{RMS}, Ripple Factor (γ), and Efficiency (η) for Half Wave Rectifier (HWR)
3. For the following circuit, find both the unknown voltages V1 and V3 using KVL in both loops, given E= 15 V, V2 = 11V, V4 = 5V



Part B

(2 Q x 3 M= 06 Marks)

4. (a) Write the formula for Ripple Factor (γ) for HWR with capacitor smoothing filter and find the value of γ if frequency is 50 Hz, R is 10 KΩ and C is 1 μF. (b) Repeat for FWR with same values.
5. Draw the graphs and equivalent circuits for all the three approximation models of a diode.

Part C

(2 Q x 4 M= 08 Marks)

6. Draw the circuit and explain the working of a 2 diode FWR in detail with figures.
7. (a) Derive the formula for V_{DC} of HWR. (b)Use the final formula to calculate V_{DC} if V_{MAX} = 10 V.