Roll No.													

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF INFORMATION SCIENCE

TEST 1

Sem AY: Odd Sem 2019-20 | **Date**: 30.09.2019

Course Code: BCA 102 | **Time**: 9:30AM to 10:30AM

Course Name: Digital Electronics | **Max Marks**: 30

Program & Sem: BCA & I | **Weightage**: 15%

Instructions:

(i) *Read the question properly and answer accordingly.*

(ii) *Question paper consists of 3 parts.*

(iii) Scientific and Non-programmable calculators are permitted.

Part A[Memory Recall Questions]

Answer the Question. Each Sub Question carries two marks. **(1Qx8M=8M)**

(C.O.NO.1)[Knowledge]

1. Convert the following:

   a. $(12345)_{10} = (?)_{16} = (?)_{8}$

   b. $(1101101111110101)_2 = (?)_{16}$

   c. $(11000000111001)_2 = (?)_{10}$

   d. $(56017)_8 = (?)_{10}$

Part B [Thought Provoking Questions]

Answer all the Questions. Each Question carries five marks. **(3Qx5M=15M)**

2. State and Prove De-Morgan's Theorems. (C.O.NO.1)[Knowledge]

3. What are Universal gates? Realize fundamental gates using universal gates

(C.O.NO.1)[Knowledge]

4. Write the Truth Table and Logic circuit using basic gates for the following expression

a. $F1 = x + y'z$ b. $F2 = x'z + xy'$

(C.O.NO.1)[Knowledge]

Part C [Problem Solving Questions]

Answer the Question. The Question carries seven marks. (1Qx7M=7M)

5. Simplify $F(A,B,C,D) = \Sigma m(0,1,2,4,5,6,8,9,10,12,13)$

using K-Map and realize the resultant expression using NAND gates only.

(C.O.NO.2)[Comprehension]

SCHOOL OF INFORMATION SCIENCE

Semester: 1
Course Code: BCA 102
Course Name: Digital Electronics
Program & Sem: BCA

Date: 30/09/2019
Time: 9:30am to 10:30am
Max Marks: 40
Weightage: 20%

Extract of question distribution [outcome wise & level wise]

Q.NO	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels			Thought provoking type [Marks allotted] Bloom's Levels			Problem Solving type [Marks allotted]			Total Marks
			K			C			A			
1	CO1	Module1		12								12
2	CO1	Module1		18								18
3	CO2	Module2					10					10
	Total Marks			30			10					40

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

[I hereby certify that All the questions are set as per the above guide lines. Srivinay]

Reviewers' Comments

SCHOOL OF INFORMATION SCIENCE

GAIN MORE KNOWLEDGE REACH GREATER HEIGHTS

SOLUTION

Semester: 1

Course Code: BCA 102

Course Name: Digital Electronics

Program & Sem: BCA

Date: 30/09/2019

Time: 9:30am to 10:30am

Max Marks: 40

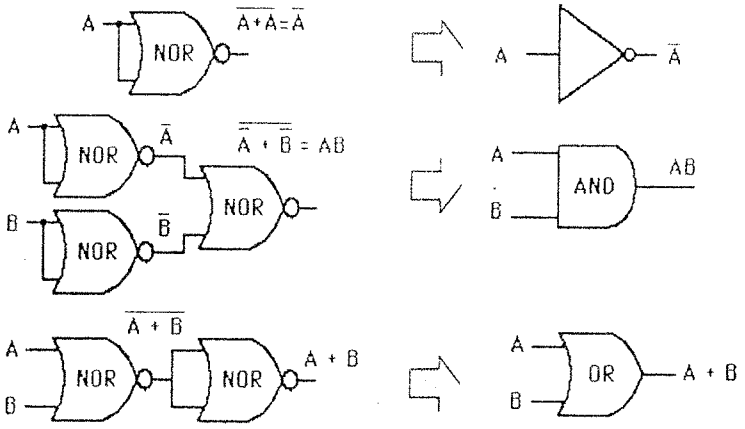
Weightage: 20%

Part A (1Q x12 M = 12 Marks)

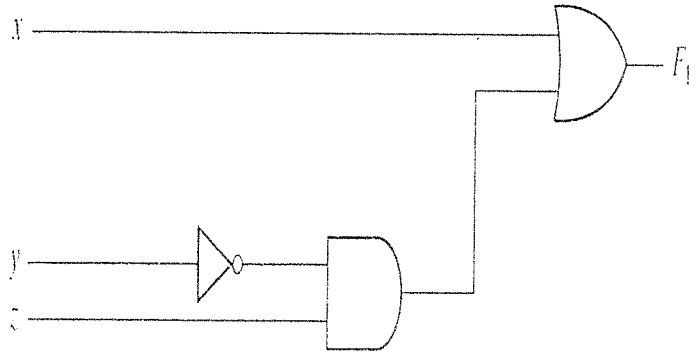
Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	a. $(3039)_{16}$ $(30071)_8$ b. (DBF5) c. $(12345)_{10}$ d. $(23567)_{10}$	3M each	15 min

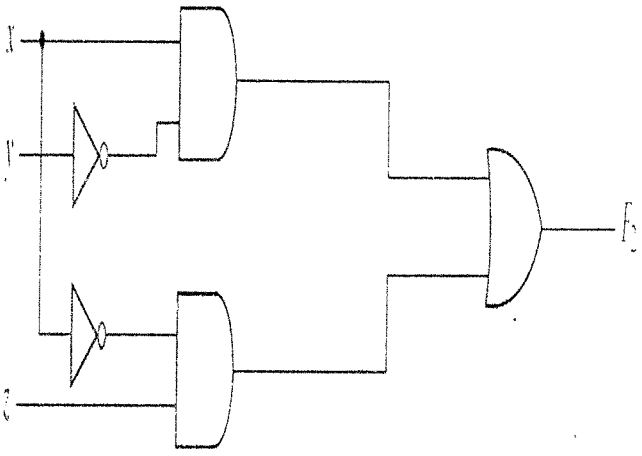
Part B (3Q x 6M = 18 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question

2.	x y $x+y$ $(x+y)'$ x' y' $x'y'$ 0 0 0 1 1 1 1 0 1 1 0 1 0 0 1 0 1 0 0 1 0 1 1 1 0 0 0 0	State- 1M Proof- 5M	5 min
3.		Defn: 1M NOR: 1M AND:2M OR: 2M	10 min
4.		T.T = 3M Circuit = 3M	15 min

x	y	z	F_1	F_2
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	0
1	1	1	1	0





(b) $F_2 = xy' + x'z$

Part C (1Q x10 M =10 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
5.	$\overline{C}.\overline{D}$ $\overline{C}.D$ $C.D$ $C.\overline{D}$ $\overline{A}.\overline{B}$ 1 1 0 1 $\overline{A}.B$ 1 1 0 1 $A.B$ 1 1 0 0 $A.\overline{B}$ 1 1 0 1 **Map Layout** $\overline{C}.\overline{D}$ $\overline{C}.D$ $C.D$ $C.\overline{D}$ $\overline{A}.\overline{B}$ 0 1 3 2 $\overline{A}.B$ 4 5 7 6 $A.B$ 12 13 15 14 $A.\overline{B}$ 8 9 11 10 **Groups** (0,1,4,5,8,9,12,13) $\overline{C}$ (0,2,4,6) $\overline{A}.\overline{D}$ (0,2,8,10) $\overline{B}.\overline{D}$ $Y = C' + A'D' + B'D$	Writing K-map – 2M Grouping – 6M Nand Implementation – 2M	15min

Roll No.													

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF INFORMATION SCIENCE

TEST – 2

Sem & AY: Odd Sem 2019-20 | **Date**: 18.11.2019

Course Code: BCA102 | **Time**: 9:30 AM to 10:30 AM

Course Name: DIGITAL ELECTRONICS | **Max Marks**: 30

Program & Sem: BCA & I | **Weightage**: 15%

Instructions:

(i) Read the question properly and answer accordingly.

(ii) Question paper consists of 3 parts.

(iii) Scientific and Non-programmable calculators are permitted.

Part A [Memory Recall Questions]

1. Answer all the Questions. Each Question carries one mark. (4Qx1M=4M)

i. There are _____ cells in a 4-variable K-map.

a. 12 b. 16 c. 18 d. 8

ii. What is the function of an enable input on a multiplexer chip?

a. To apply V_{cc}
b. To connect ground
c. To active the entire chip
d. To active one half of the chip

iii. How many select lines would be required for a 32-line-to-1-line multiplexer?

a. 2 b. 4 c. 8 d. 5

iv. The prime implicant which has at least one element that is not present in any other implicant is known as _____

a. Essential Prime Implicant
b. Implicant
c. Complement
d. Prime Complement

(C.O.NO.1) [Knowledge]

Part B [Thought Provoking Questions]

Answer both the Questions. Each Question carries six marks. (2Qx6M=12M)

(C.O.NO.3) [Application]

2. Show how 8:1 Multiplexer can be obtained by using only 2:1 Multiplexer.

3. With a neat block diagram, truth table and logic circuit. Explain the working of a Half Adder and Full Adder.

Part C [Problem Solving Questions]

Answer both the Questions. (2Q=14M)

(C.O.NO.2) [Application]

4. Simplify F (A,B,C,D) = Σm(0,1,2,3,10,11,12,13,14,15) using QM method. Implement the resultant expression using NAND gates only. [10 M]

5. Simplify F (A,B,C,D) = Σm(0,2,4,6,8,9,10,12,14) + d(1,5,11,13) using K-map [4 M]

SCHOOL OF INFORMATION SCIENCE

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

Semester: 1
Course Code: BCA 102
Course Name: Digital Electronics
Program & Sem: BCA

Date: 18/11/2019
Time: 9:30am to 10:30am
Max Marks: 30
Weightage: 15%

Extract of question distribution [outcome wise & level wise]

Q.NO	C.O.NO	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	A	
1	CO1	Module2,3	4			4
2	CO3	Module3			12	12
3	CO2	Module2			14	14
	Total Marks		4	00	26	30

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

SCHOOL OF INFORMATION SCIENCE

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

SOLUTION

Semester: 1
Course Code: BCA 102
Course Name: Digital Electronics
Program & Sem: BCA

Date: 30/09/2019
Time: 9:30am to 10:30am
Max Marks: 40
Weightage: 20%

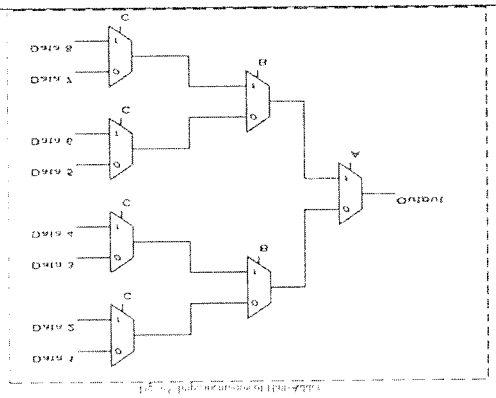
Part A

(4Q x1 M = 4 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
1	i. 16 ii. To active the entire chip iii. 5 iv. Essential Prime Implicant	1M each	5 min

Part B

(2Q x 6M = 12 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
2.		Expression: 2M Diagram- 4M	10 min
3.	 Table 4-3 Half Adder x y | C S 0 0 | 0 0 0 1 | 0 1 1 0 | 0 1 1 1 | 1 0	Half Adder 3M Full Adder 3M	10 min

Part C

Q No	Solution	Scheme of Marking	Max. Time required for each Question
4.	Prime Implicants A'B', B'C, AC, AB EPI Y= A'B' + AC +AB	PI Table : 4M EPI Table: 3M NAND circuit: 4M	25 min
5.	**Map** C.D C.D C.D C.D A.B 1 x 0 1 A.B 1 x 0 1 A.B 1 x 0 1 A.B 1 1 x 1 **Map Layout** C.D C.D C.D C.D A.B 0 1 3 2 A.B 4 5 7 6 A.B 12 13 15 14 A.B 8 9 11 10 **Groups** (0,2,4,6,8,10,12,14) D (0,1,4,5,8,9,12,13) C y = D' + C'	Grouping: 2M Writing Expression: 2M	10 min

Roll No												

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF INFORMATION SCIENCE

END TERM FINAL EXAMINATION

Semester: Odd Semester: 2019-20 | **Date**: 03 January 2020

Course Code: BCA 102 | **Time**: 1:00 PM to 4:00 PM

Course Name: DIGITAL ELECTRONICS | **Max Marks**: 100

Program & Sem: BCA & I | **Weightage**: 50%

Instructions:

(i) Read all questions carefully and answer accordingly.

Part A [Memory Recall Questions]

Answer all the Questions. Each Question carries 8 marks. (2Qx8M=16M)

1. Convert the following: (C.O.No.1) [Knowledge]

   i. $(12345)_{10} = (?)_{16} = (?)_{8}$

   ii. $(1101101111110101)_{2} = (?)_{16}$

   iii. $(11000000111001)_{2} = (?)_{10}$

   iv. $(56017)_{8} = (?)_{10}$

2. a) State and Prove De-Morgan's theorem. (C.O.No.1) [Knowledge]

   b) Realize Basic gates using Universal gates.

Part B [Thought Provoking Questions]

Answer all the Questions. Each Question carries 10 marks. (6Qx10M=60M)

3. With a neat block diagram, truth table and logic circuit. Explain the working of a Half Adder and Full Adder. (C.O.No.3) [Comprehension]

4. Show how 8:1 Multiplexer can be obtained by using only 2:1 Multiplexer along with the boolean expression (C.O.No.3) [Application]

5. With a neat logic diagram, explain the working of a BCD to Excess3 code converter. (C.O.No.3) [Comprehension]

6. What is the difference between a Latch and a Flip-flop? Show the state transition diagram of SR, D, JK, and T Flip-flops. (C.O.No.3) [Application]

7. With a neat logic circuit, logic symbol, and characteristic table, explain the working of negative edge triggered JK-Flip-flop. (C.O.No.3) [Comprehension]

8. With a neat logic diagram, explain the working of a 3-bit Ripple counter. (C.O.No.3) [Comprehension]

Part C [Problem Solving Questions]

Answer both the Questions. Each Question carries 12 marks. (2Qx12M=24M)

9. a) Simplify F(A,B,C,D) = Σm(0,1,2,4,5,6,8,9,10,12,13) using K-Map and realize the resultant expression using NAND gates only. (C.O.No.2) [Application]

b) Simplify F (A,B,C,D) = Σm(0,2,4,6,8,9,10,12,14) + d(1,5,11,13) using K-map

10. Simplify F (A,B,C,D) = Σm(0,1,2,3,10,11,12,13,14,15) using QM method. Implement the resultant expression using NAND gates only. (C.O.No.2) [Application]

SCHOOL OF INFORMATION SCIENCE

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

END TERM FINAL EXAMINATION

Extract of question distribution [outcome wise & level wise]

Q.NO.	C.O. NO (% age of CO)	Unit/Module Number/Unit /Module Title	Memory recall type [Marks allotted] Bloom's Levels	Thought provoking type [Marks allotted] Bloom's Levels	Problem Solving type [Marks allotted]	Total Marks
			K	C	A	
Part A Q. No1	**C.O. No.1**	Module1	8			8
Part A Q. No2	**C.O. No.1**	Module1	8			8
Part B Q. No3	**C.O. No.3**	Module 3		10		10
Part B Q. No4	**C.O. No.3**	Module 3			10	10
Part B Q. No5	**C.O. No.3**	Module 3		10		10
Part B Q. No6	**C.O. No.3**	Module 3			10	10
Part B Q. No7	**C.O. No.3**	Module 3		10		10
Part B Q. No8	**C.O. No.3**	Module 3		10		10
Part C Q. No9	**C.O. No.2**	Module 2			12	10

Part C Q. No10	**C.O. No.2**	Module 2			12	10
	Total Marks		16	40	44	100

K =Knowledge Level C = Comprehension Level, A = Application Level

Note: While setting all types of questions the general guideline is that about 60%

Of the questions must be such that even a below average students must be able to attempt, About 20% of the questions must be such that only above average students must be able to attempt and finally 20% of the questions must be such that only the bright students must be able to attempt.

I hereby certify that all the questions are set as per the above guidelines.

Faculty Signature:

Reviewer Comment:

16 Marks only given for knowledge level. Discussed with QP setter. Informed me that students are well Trained to solve the Part-C prob-solving questions.

27/12/19.

Format of Answer Scheme

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

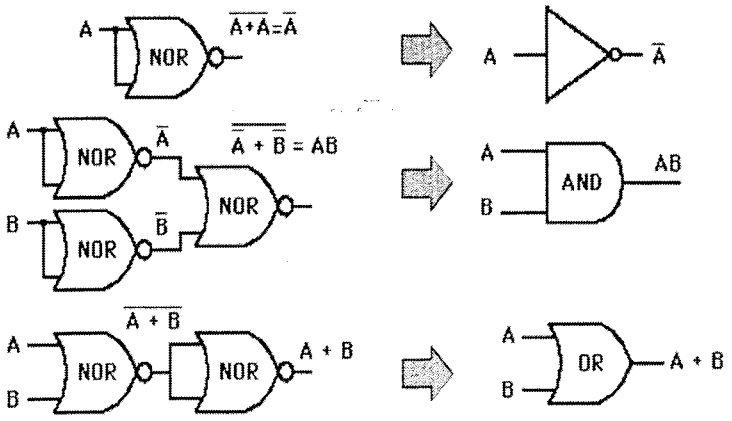
SCHOOL OF ENGINEERING

SOLUTION

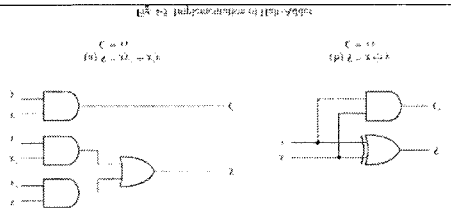
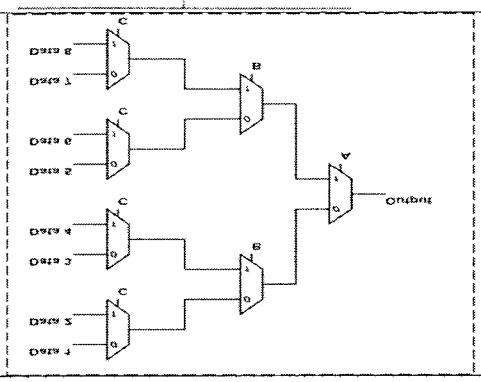
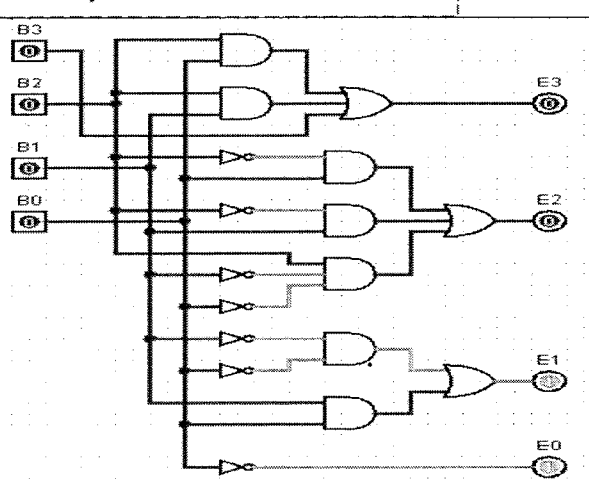
Semester: Odd sem 2019-20
Course Code: BCA 102
Course Name: Digital Electronics
Program & Sem: BCA 1st sem

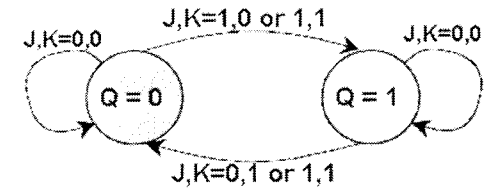
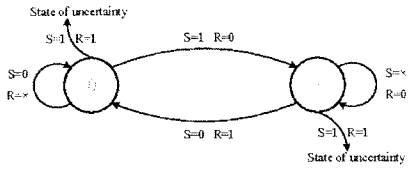
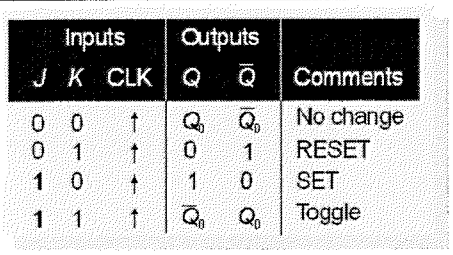
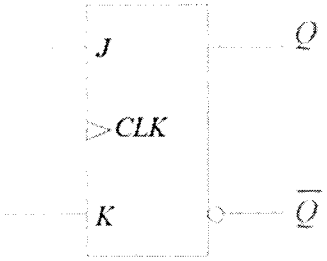
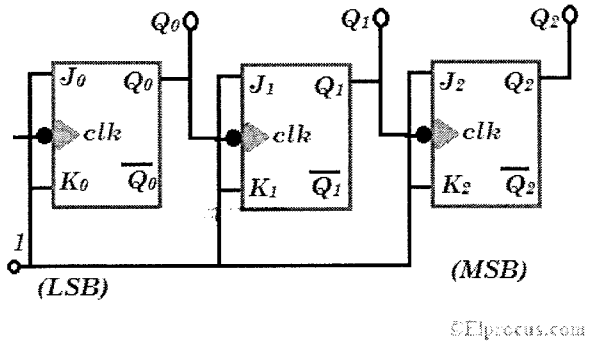
Date: 03 Jan 2020
Time: 1:00pm to 4:00pm
Max Marks: 100
Weightage: 50%

Part A (2Q x 10M = 20Marks)

<table>
<tr><th>Q No</th><th>Solution</th><th>Scheme of Marking</th><th>Max. Time required for each Question</th></tr>
<tr><td>1</td><td>a. $(3039)_{16}$ $(30071)_8$
b. (DBF5)
c. $(12345)_{10}$
d. $(23567)_{10}$</td><td>2M EACH</td><td>10min</td></tr>
<tr><td>2.a)</td><td>
<table>
<tr><th>x</th><th>y</th><th>x + y</th><th>(x + y)′</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td></tr>
</table>
<table>
<tr><th>x′</th><th>y′</th><th>x′y′</th></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
</table>
</td><td>4M</td><td>20min</td></tr>
<tr><td>2.b)</td><td> 
</td><td>4M</td><td></td></tr>
</table>

Part B (6Q x 10M = 60 Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
3	 **Table 4-3** *Half Adder* x y | C S 0 0 | 0 0 0 1 | 0 1 1 0 | 0 1 1 1 | 1 0	Half adder – 5M Full Adder – 5M	20min
4		Boolean expression – 4M Circuit—6M	10min
5	 **Excess-3 code** can be derived from **BCD code** by adding **3** to each number. For example, Decimal number 12 is represented as 0001 0010 in **BCD**. If we add **3** that is to add 0011 0011 then the corresponding **Excess-3 code** is 0100 0101.	Truth Table –4M K-map – 3M Circuit – 3M	25min

6	  Fig. 5. The state diagram of SR flip-flop circuit (CP = 1). *Latch and Flip-flop are used to store 1 bit. But flipflop is controlled by a clock * Latch is a trnasparent circuit.	Difference- 2M Each flip-flop transition—2M	20min
7	 	Inputs			Outputs		
---	---	---	---	---	---
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle |  Explaination of truth table is required	Logic circuit – 2M Logic symbol – 2M Characteristic table – 3M Explanation –3M	15min
8	 Write the 3 bit truth table and explanation of circuit	Circuit—5M Table –2M Explanation – 3M	15min

Part C (2Q x 12M = 24Marks)

Q No	Solution	Scheme of Marking	Max. Time required for each Question
9.a)	$\overline{C}.\overline{D}$ $\overline{C}.D$ $C.D$ $C.\overline{D}$ $\overline{A}.\overline{B}$ 1 1 0 1 $\overline{A}.B$ 1 1 0 1 $A.B$ 1 1 0 0 $A.\overline{B}$ 1 1 0 1 **Map Layout** $\overline{C}.\overline{D}$ $\overline{C}.D$ $C.D$ $C.\overline{D}$ $\overline{A}.\overline{B}$ 0 1 3 2 $\overline{A}.B$ 4 5 7 6 $A.B$ 12 13 15 14 $A.\overline{B}$ 8 9 11 10 **Groups** (0,1,4,5,8,9,12,13) $\overline{C}$ (0,2,4,6) $\overline{A}.\overline{D}$ (0,2,8,10) $\overline{B}.\overline{D}$ $y = C' - A'D' - B'D'$	Writing K-map – 2M Grouping – 2M Nand Implementation – 2M	20min
9.b)	**Map** | | C.D | C.D | C.D | C.D | | A.B | 1 | x | 0 | 1 | | A.B | 1 | x | 0 | 1 | | A.B | 1 | x | 0 | 1 | | A.B | 1 | 1 | x | 1 | **Map Layout** | | C.D | C.D | C.D | C.D | | A.B | 0 | 1 | 3 | 2 | | A.B | 4 | 5 | 7 | 6 | | A.B | 12 | 13 | 15 | 14 | | A.B | 8 | 9 | 11 | 10 | **Groups** | (0,2,4,6,8,10,12,14) | D | | (0,1,4,5,8,9,12,13) | C | Y=D' +C'	Writing K-map – 2M Grouping – 4M	
10	Prime Implicants A'B', B'C, AC, AB EPI Y= A'B' + AC +AB	PI Table : 5M EPI Table: 4M NAND circuit: 3M	25min