Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

Mid - Term Examinations – October 2025

Date: 10-10-2025 **Time:** 11.45am to 01.15pm

School: SOE	**Program:** Electronics and Communication Engineering	
Course Code : ECE3043	**Course Name:** Mixed Signal Circuit Design	
Semester: V	**Max Marks**: 50	**Weightage**: 25%

CO - Levels	CO1	CO2	CO3	CO4	CO5
Marks	12	24	14		

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **5Q x 2M=10M**

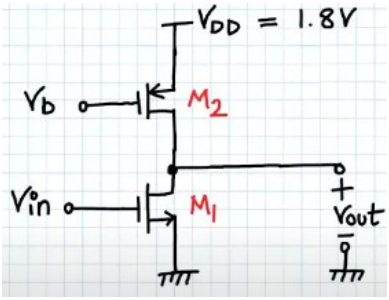
1	In MOSFET amplifier, a small change within gate voltage will generate a large change within drain current. For an NMOS, 3V is applied between gate and source and the threshold voltage is 0.8V. Calculate the value of V_{DS} for MOSFET to operates in saturation.	**2 Marks**	**L1**	**CO1**
2	A cascade amplifier is a two-port network designed with amplifiers which are connected in series when every amplifier transmits its output to the second amplifiers input in a daisy chain. Mention the advantages and disadvantages of cascade amplifier.	**2 Marks**	**L2**	**CO2**
3	Compensation techniques are used to improve stability and prevent oscillation by controlling the frequency response. List the advantages and disadvantages of pole zero compensation.	**2 Marks**	**L1**	**CO2**
4	A Schmitt trigger is a comparator with positive feedback that creates hysteresis, using two distinct thresholds. In a Schmitt circuit, R_2=100 Ohm, R_1=50KOhm, V_{ref} = 0V, V_i=1V_{pp} sinewave and saturation voltage ± 14V. Determine the hysteresis voltage.	**2 Marks**	**L2**	**CO3**
5	A PLL is a control system that generates an output signal whose phase	**2 Marks**	**L1**	**CO3**

		is fixed relative to the phase of an input signal. Mention the purpose of the phase detector and LPF in PLL.			

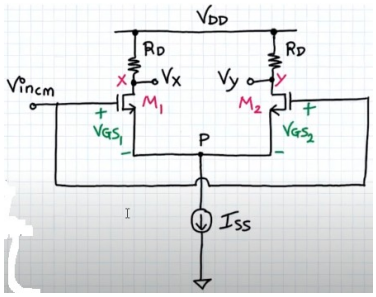
Part B

Answer the Questions. **Total Marks 40M**

6.	**a.**	MOSFET is a type of FET with an insulated gate that is assembled by the controlled oxidation of that semiconductor. Explain the Drain and transfer characteristics of N Channel Enhancement type MOSFET. Also mention the difference between N-Channel and P-Channel MOSFET.	**10 Marks**	**L2**	**CO1**
		Or			
7.	**a.**	MOSFET is known as a voltage-driven device and requires simple gate control circuit. Mention the MOSFET current equation in triode region, saturation region, and cut-off-region.	**10 Marks**	**L2**	**CO1**

8.	**a.**	A common-source amplifier is used for high voltage amplification and high input impedance. Derive the expression for voltage gain and output impedance for Common Source Amplifier with PMOS as Load.	**10 Marks**	**L3**	**CO2**
		Or			
9.	**a.**	The CS amplifier provides the voltage gain of 10 with a bias current of 0.5mA. Assume $\lambda_1=0.1V^{-1}$, $\lambda_2=0.15V^{-1}$, $\mu_nC_{ox}=200\mu A/V^2$, $\mu_pC_{ox}=100\mu A/V^2$, $V_{th}=0.4V$ for NMOS and $V_{th}=-0.4V$ for PMOS. Calculate (a) the required $(w/L)_1$ (b) If $(W/L)_1=20/0.18$, calculate the value of V_B. 	**10 Marks**	**L3**	**CO2**

10.	**a.**	A differential amplifier's ability is to reject common signals to both inputs, known as common-mode signals, rather than amplifying them. In a MOS differential amplifier as shown in figure, $V_{inCM}=1V$, $I_{SS}=1mA$ and $R_D=1K\Omega$. Evaluate the minimum allowable supply voltage if the transistors will remain in saturation. Assume V_{th} for NMOS = 0.5V.	**10 Marks**	**L3**	**CO2**

					
Or					
11.	**a.**	An astable multivibrator, also called a free-running multivibrator, is a circuit that continuously produces square waves or pulses without the use of an external trigger. Explain the working of Astable Multivibrator with output waveform.	**10 Marks**	**L2**	**CO2**

12.	**a.**	A phase detector is a circuit that compares two input signals and generates an output signal that reflects the phase difference between them. Analog Phase detector in PLL using input and output waveform for ϕ=0°, ϕ=90°, ϕ=180°.	**10 Marks**	**L3**	**CO3**
Or					
13.	**a.**	PLL generates an output frequency which is based on a reference input clock. The output frequency can be either higher or lower than the input. Explain the working of Frequency translation in PLL with figure.	**10 Marks**	**L3**	**CO3**