



PRESIDENCY UNIVERSITY

BENGALURU

Roll No.														
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Mid - Term Examinations – October 2025

Date: 08-10-2025

Time: 02.00pm to 03.30pm

School: SOE	Program: Electronics and Communication Engineering		
Course Code : ECE2021	Course Name: Digital Electronics		
Semester: III	Max Marks: 50	Weightage: 25%	

CO - Levels	CO1	CO2	CO3	CO4	CO5	CO6
Marks	12	14	12	-	-	12

Instructions:

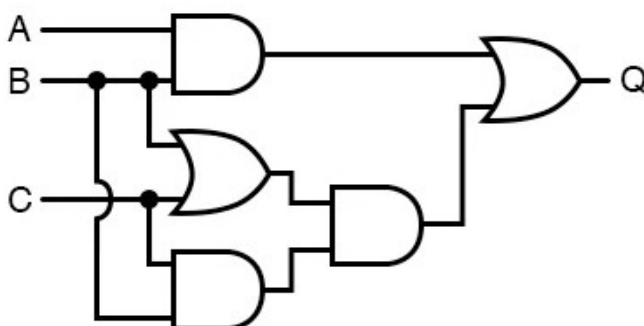
- (i) Read all questions carefully and answer accordingly.
- (ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks.

5Q x 2M=10M

1	Illustrate the 7 th and 14 th Minterm for the 4 bit resolution	2 Marks	L3	CO1
2	Implement the two input EX-NOR logic using NOR gate.	2 Marks	L3	CO2
3	Estimate the Boolean Function of the CARRY output for the Half adder circuit	2 Marks	L3	CO3
4	Identify the equivalent gray code for the decimal numbers 0,1,3,4,7	2 Marks	L2	CO2
5	Utilize the below Logic Diagram to drive the Truth Table.	2 Marks	L3	CO6



Part B

Answer the Questions.

Total Marks 40M

6.	a.	<p>Solve the following function as a sum of min-terms and as a product of max-terms with logic diagram</p> <p>i. $F(A, B, C, D) = B'D + A'D + BD$</p> <p>ii. $Y = (CD + B'C + BD')(B + D)$</p> <p>iii. $Z = BD' + ACD' + AB'C + A'C'$</p> <p>iv. $P = (C' + D)(B + C')$</p>	10 Marks	L3	C01
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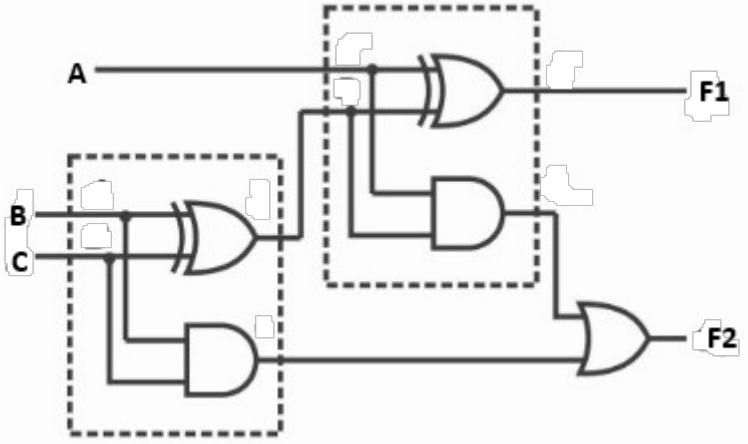
Or

7.	a.	<p>Employ the NAND gate for the following Boolean functions</p> <p>(a) $F(w, x, y, z) = \sum m(0, 2, 5, 7, 8, 10, 12, 13, 14, 15)$</p> <p>(b) $F(A, B, C, D) = \sum m(0, 2, 3, 5, 7, 8, 10, 11, 14, 15)$</p>	10 Marks	L3	C01
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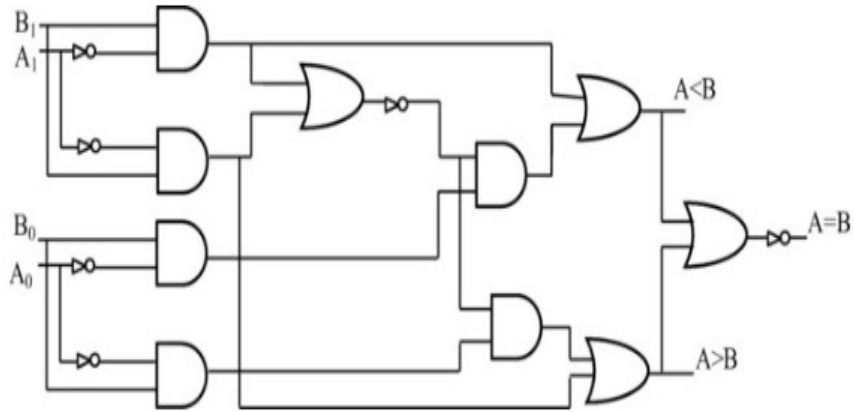
8.	a.	<p>Develop the optimized Boolean Function for the following</p> <p>i. $Y = \sum m(1, 2, 3, 7, 8, 10, 12, 13, 15)$</p> <p>ii. $F = W'Z + XZ + X'Y + WX'Z$</p>	10 Marks	L2	C02
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Or

9.	a.	<p>Implement the following Boolean function F, together with the don't-care conditions d.</p> <p>(i) $F(W, X, Y, Z) = \sum (0, 1, 2, 7, 9, 11) + d = \sum (3, 4, 8)$</p> <p>(ii) $F(A, B, C) = A'C + A'B + AB'C + BC$</p>	10 Marks	L3	C02
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10.	a.	<p>Examine the following logic diagram to identify the design statement</p> 	10 Marks	L4	C06
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Or

11.	a.	<p>Analysis the below circuit to prove that the digital circuit is a 2 bit comparator</p> 	10 Marks	L4	C06
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12.	a.	<p>Apply the concept of truth table to draw the logic circuit diagram of a full adder using basic logic gates.</p>	10 Marks	L3	C03
Or					
13.	a.	<p>Develop the Logical Circuit which has a 3-bit digital system which rings a buzzer whenever the number of ones in an input combination is ODD.</p>	10 Marks	L3	C03