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PRESIDENCY UNIVERSITY

BENGALURU

Mid - Term Examinations – October 2025

Date: 09-10-2025

Time: 09.30am to 11.00am

School: SOCSE / SOE	Program: BTECH (CSE)	
Course Code : ECE2022	Course Name: DIGITAL DESIGN	
Semester: I	Max Marks:50	Weightage:25%

CO - Levels	CO1	CO2	CO3	CO4	CO5	CO6
Marks	10	15	25	NA	NA	NA

Instructions:

- (i) Read all questions carefully and answer accordingly.
- (ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks.

5Q x 2M=10M

1	Find the equivalent binary number representation of the given decimal number 16.125 ?	2 Marks	L2	CO1																																				
2	In the given Truth Table A,B & C are input literals(variables) and Y is output literal. In terms of input literals list out the Max terms: <table border="1"><thead><tr><th>A</th><th>B</th><th>C</th><th>Y</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></tbody></table>	A	B	C	Y	0	0	0	1	0	0	1	1	0	1	0	0	0	1	1	0	1	0	0	1	1	0	1	0	1	1	0	0	1	1	1	1	2 Marks	L2	CO1
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3	State Associative Law and Sketch the logic circuit using two input basic gate and Tabulate the Truth Table:	2 Marks	L2	CO1																																				
4	Restructure the OR gate logic using NOR gate only:	2 Marks	L2	CO1																																				
5	Predict SoP Equation for the given truth table: <table border="1"><thead><tr><th>A</th><th>B</th><th>Y</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></tbody></table>	A	B	Y	0	0	0	0	1	0	1	0	0	1	1	1	2 Marks	L2	CO1																					
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Part B

Answer the Questions.

Total Marks 40M

6.	a.	<p>The given Standard Boolean function is, $F(W,X,Y,Z) = W'X'Y' + WY'Z' + X'YZ' + W'XZ + XY'Z.$</p> <p>i) Convert the function "F" into Canonical form. ii) Using K-map, Simplify into minimum SOP function.</p>	10 Marks	L2	CO2
	b.	<p>Determine the minimum SoP (using K Map) for the given Boolean function $F = \Sigma(m_2, m_3, m_4, m_6, m_8, m_9, m_{14}, m_{15})$ Also draw the logic circuit using NAND gate only:</p>	10 Marks	L3	CO2, CO3

Or

7.	a.	<p>i) Obtain the canonical form for the following standard function: $F = (A \cdot B' \cdot C') + (A \cdot B \cdot C \cdot D) + (A' \cdot B \cdot C' \cdot D) + (A' \cdot B' \cdot C \cdot D)$ $F = (B + C' + D') \cdot (A' + B' + D) \cdot (A + B' + C')$</p> <p>ii) Determine all the Selective Prime Implicants, for the Boolean function: $F(A,B,C,D) = \Sigma m(1,2,3,4,5)$</p>	10 Marks	L2	CO2
	b.	<p>Determine the minimum SoP (using K Map) for the given Boolean function $F(A,B,C,D) = \Sigma(m_0, m_1, m_4, m_8, m_9, m_{15}) + DC(6,14).$ Also draw the logic circuit using NAND gate only:</p>	10 Marks	L3	CO2, CO3

8.	a.	<p>Predict Half Adder Truth Table, and Determine the Logic Circuit by using: i) Basic gates: ii) EXOR, and AND gates:</p>	15 Marks	L3	CO3
	b.	<p>Sketch the Full Adder circuit using minimum NAND gate:</p>	5 Marks	L2	CO3

Or

9.	a.	<p>Design a combinational circuit for Binary Addition of three 1-bit number (Full Adder) using minimum number of Two input ExOR gate, Two input AND gate or Two input OR gate:</p>	15 Marks	L3	CO3
	b.	<p>Sketch the Half Subtractor logic circuit using minimum NAND gates:</p>	5 Marks	L2	CO3