ROLL NO	

PRESIDENCY UNIVERSITY, BENGALURU
SCHOOL OF ENGINEERING

Max Marks: 40 | Max Time: 120 Mins | Weightage: 40 %

ENDTERM FINAL EXAMINATION

I Semester AY 2017-18 Course: **ECE/EEE 201 ANALOG ELECTRONICS** 19 DECEMBER 2017

Instructions:

i. Write legibly

ii. Scientific and non-programmable calculators are permitted

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Part A

[4 Q x 4 M= 16 Marks]

1. On what basis the power amplifiers are classified? List only the types of power amplifiers.

2. Give a comparison table for the Push-Pull and Complementary Symmetry Class-B amplifiers.

3. Using the voltage and current equivalencies of a two-port network, obtain different h-parameters (**Hint: Use Two-Port equations**).

4. Briefly discuss the operation of an n-channel JFET by drawing its construction diagram with proper voltage sources and its characteristics curve.

Part B

[2 Q x 7 M= 14 Marks]

5. Show that the Class-A Series Fed power amplifier has a maximum power efficiency of 25%.

6. With the help of a neat circuit diagram, explain the working of Heartley Oscillator.

Part C

[1 Q x 10 M= 10 Marks]

7. The typical h-parameter values of a Common Emitter amplifier is given as h_{ie} = 1100 Ω, h_{re} = 2.5 x 10^{-4}, h_{fe} = 50, h_{oe} = 24 μA / V. If the load resistance R_L = 20K and the source resistance R_S = 4K, find A_I, A_{IS}, R_i, A_V, A_{VS}.

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Max Marks: 20 | Max Time: 60 Mins | Weightage: 20 %

TEST 2

I Semester AY 2017-2018 | ***Course:*** **ECE/EEE 201 ANALOG ELECTRONICS** | 27-OCT-2017

Instructions:

i. Write legibly
ii. Scientific and non programmable calculators are permitted

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Part A

(1Q x 8 M= 08 Marks)

1) Explain with a neat diagram voltage divider bias circuit for Exact analysis.

Part B

(1Q x 7M= 07 Marks)

2) Draw a double diode clipper which limits at two independent levels and explain its Working.

Part C

(1Q x5 M= 05 Marks)

3) For the fixed bias circuit, RB=50kΩ, Rc=500Ω, Vcc=10 V. Find the coordinates of the operating points. Draw the DC load line and locate the operating points on the DC load line. Assume silicon transistor with β=50 and VBE=0.7v.

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Max Marks: 20 | Max Time: 60 Mins | Weightage: 20 %

TEST 1

I Semester 2017-2018 | Course: **ECE / EEE 201 Analog Electronics** | 16 September 2017

Instructions:

i. Write legibly
ii. Scientific and non-programmable calculators are permitted.

Part A (3 Q x 2 M = 6 Marks)

1. Briefly explain with a neat sketch the "Hall Effect".
2. Plot and label the V-I characteristics for a Ge and Si diode.
3. Define the Diffusion Capacitance and Transition Capacitance.

Part B (1 Q x 6 M = 6 Marks)

4. Find I and V in the four circuits shown in Figure - 1 below using the constant voltage drop (simplified) model with $V_{Th} = V_\gamma = V_K = 0.7\ V$.

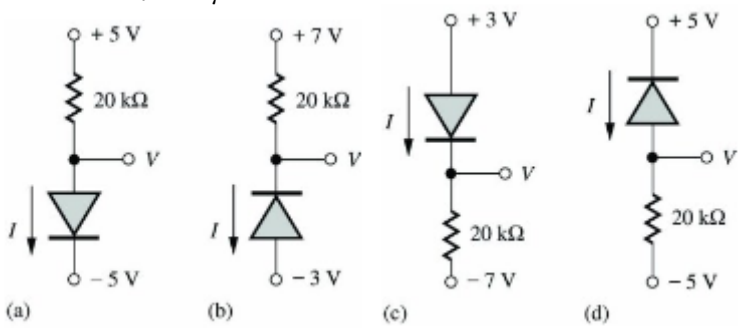

Figure – 1

Part C (1 Q x 8 M = 8 Marks)

5. With a neat circuit diagram and the corresponding waveform, explain the working principle of a Full Wave Rectifier (with 2 diodes) and derive the following formulae:
   (a) I_{dc} (b) I_{rms} (c) Ripple Factor.