Roll No.											

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – December 2025

Date: 13 – 12- 2025 **Time:** 09:30am – 12:30pm

School: SOE	**Program:** Electronics and Communication Engineering	
Course Code: ECE2021	**Course Name:** Digital Electronics	
Semester: III	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**	**CO6**
Marks	**14**	**14**	**24**	**24**	**10**	**14**

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

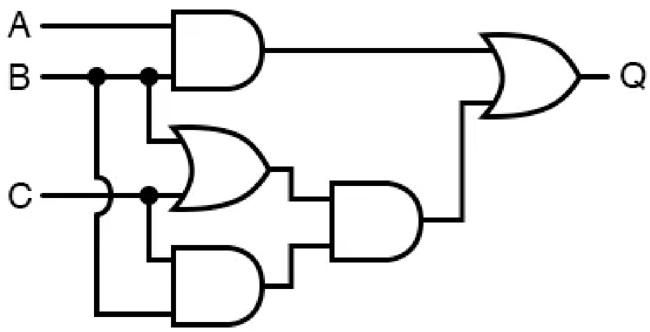
Answer ALL the Questions. Each question carries 2marks. 10Q x 2M=20M

1.	Illustrate the 9th and 12th Minterm for the 4 bit resolution.	**2 Marks**	**L3**	**CO1**
2.	Estimate the decimal equivalence for the binary number 1000.111.	**2 Marks**	**L3**	**CO1**
3.	Implement the two input EX-NOR logic using NOR gate.	**2 Marks**	**L3**	**CO2**
4.	Identify the equivalent gray code for the decimal numbers 0,2,4,8,11.	**2 Marks**	**L2**	**CO2**
5.	Estimate the Boolean Function of the CARRY output for the Full adder circuit.	**2 Marks**	**L3**	**CO3**
6.	Summarize the truth table for 2 bit Subtractor circuit.	**2 Marks**	**L2**	**CO3**
7.	Derive the Excitation table for SR flip flop.	**2 Marks**	**L3**	**CO4**
8.	Differentiate between the Sequential and Combination Circuit.	**2 Marks**	**L3**	**CO4**

9.	Utilize the given truth table to derive the Boolean equation in Canonical Form.	**2 Marks**	**L3**	**CO6**

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

10.	Utilize the below Logic Diagram to drive the Truth Table.	**2 Marks**	**L3**	**CO6**



Part B

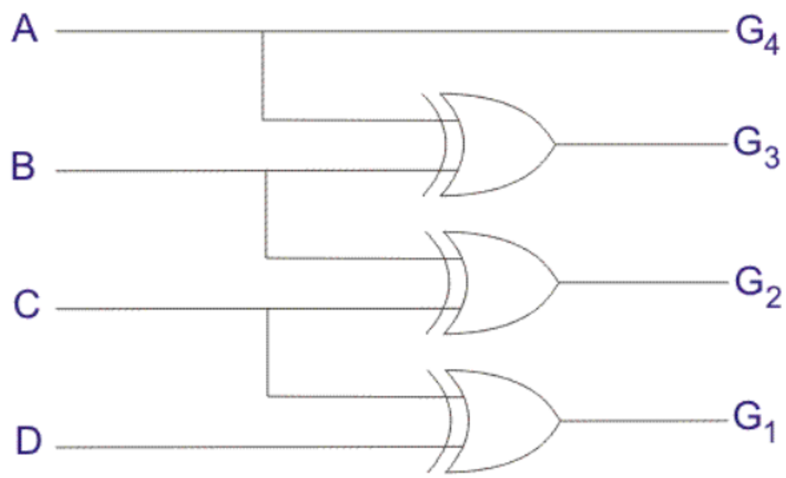
Answer the Questions. **Total Marks 80M**

11.	**a.**	Employ the NAND gate for the following Boolean functions. (a) $F(w, x, y, z) = \sum m\ (0, 2, 5, 7, 8, 10, 12, 13, 14, 15)$ (b) $F(A, B, C, D) = \sum m\ (0, 2, 3, 5, 7, 8, 10, 11, 14, 15)$	**10 Marks**	**L3**	**CO1**
	b.	Develop the optimized Boolean Function for the following. i. $Y= \sum m\ (1,2,3,7, 8,10,12,13,15)$ ii. $F = W'Z + XZ + X'Y + WX'Z$	**10 Marks**	**L2**	**CO2**
		Or			
12.	**a.**	Solve the following expression using Boolean Theorem. i. $AB + (AC)' + AB'C(AB + C)= 1$ ii. $((XY' + XYZ)' + X(Y + XY'))' = 0$	**10 Marks**	**L3**	**CO1**
	b.	Identity the optimized Standard forms (SOP & POS) of Boolean Function for the following. $F\ (w, x, y, z) = \sum\pi\ (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$	**10 Marks**	**L3**	**CO2**

13.	**a.**	Design the 3:8 Decoder using basic logic gates.	**10 Marks**	**L3**	**CO3**
	b.	Implement the Function $F = \sum m\ (0,3,5,10,11,12,13,15)$ using Multiplexer.	**10 Marks**	**L3**	**CO3**

		Or			
14.	**a.**	Design the adder circuit that adds 3 bits to generate Sum and Carry .	**5 Marks**	**L3**	**CO3**
	b.	Design the two bit comparator to indicate whether it is Lesser, Greater or Equal.	**15 Marks**	**L3**	**CO3**

15.	**a.**	Discuss about the types of Sift Registers with necessary diagram and tables.	**20 Marks**	**L3**	**CO4**
		Or			
16.	**a.**	Develop the synchronous sequential circuit that cyclically counts from 7 to 0 using the JK-Flip Flop and trigger the circuit using a positive edge clock pulse.	**20 Marks**	**L3**	**CO4**

17.	**a.**	Develop the HDL code for the design of 2 bit Subtractor to give DIFFERENCE and BORROW.	**10 Marks**	**L3**	**CO5**
	b.	Develop the HDL code for the design of 3 bit Adder to give SUM and CARRY.	**10 Marks**	**L3**	**CO5**
		Or			
18.	**a.**	Analyze the following circuit to find the design statement. 	**20 Marks**	**L4**	**CO6**