Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – December 2025

Date: 17 – 12- 2025 **Time:** 01:00pm – 04:00pm

School: SOE	**Program:** B. Tech	
Course Code: ECE3122	**Course Name:** Microelectronics	
Semester: V	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	CO1	CO2	CO3	CO4	CO5	CO6
Marks	14	12	12	24	14	24

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1.	Compute the concentration of valence electrons in a unit cell of crystalline silicon where the edge of the unit cell is a_0 = 5.43 A^0.	2 Marks	L1	CO1
2.	List the limitations of Bond Model.	2 Marks	L1	CO1
3.	The current in a PN junction diode is measured to be 3 μA for a forward bias voltage of V_D= 600 mV. Find the saturation current I_0.	2 Marks	L1	CO2
4.	What is the role of the depletion region in a photodiode?	2 Marks	L1	CO3
5.	What is the Early effect in a BJT Transistors?	2 Marks	L1	CO4
6.	Mention any two importance of MOS Transistor over BJT for IC fabrication.	2 Marks	L1	CO4
7.	In a common-source amplifier with a DC drain current ID = 100 μA and RD = 25 KΩ. The MOS device characteristics are Vth = 1 V, μnCox = 50 μA/V^2, and W/L = 50/2. Using the two-port model, find the intrinsic transconductance of the amplifier.	2 Marks	L1	CO5
8.	Differentiate between Enhancement mode MOSFETs and Depletion mode MOSFETs.	2 Marks	L1	CO5
9.	Draw the schematic diagram of DRAM memory cell.	2 Marks	L1	CO6
10.	Implement 4:1 Mux using Transmission Gates.	2 Marks	L1	CO6

Part B

Answer the Questions. **Total Marks 80M**

<table>
<tr><td>11.</td><td>a.</td><td>Illustrate the concept of donor and acceptor compensation in semiconductors, and how the presence of both types of impurities influences electrical neutrality and the carrier concentration in a doped semiconductor.</td><td>10 Marks</td><td>L2</td><td>CO1</td></tr>
<tr><td></td><td>b.</td><td>An IC diode is designed to have a room-temperature saturation current of Io = 5 X 10^{-17}Amps for a particular application. The fabrication process results in the device dimensions and physical parameters listed below.
<table>
<tr><td>Wp = 0.5 μm</td><td>Na = 2.5 x 10^17 cm-3</td><td>Dn = 14 cm2 s-1</td></tr>
<tr><td>Wn = 1 μm</td><td>Nd = 4 x 10^18 cm-3</td><td>Dp = 10 cm2 s-1</td></tr>
</table>
a. Assuming that the short-base diode analysis applies, find the Area A of the diode.
b. Find the current and the minority carrier concentrations at the edges of the depletion region for a forward bias of 720 mV.</td><td>10 Marks</td><td>L3</td><td>CO2</td></tr>
<tr><td colspan="6">Or</td></tr>
<tr><td>12.</td><td>a.</td><td>Derive an expression for diffusion current density in p-region with necessary analysis.</td><td>10 Marks</td><td>L2</td><td>CO1</td></tr>
<tr><td></td><td>b.</td><td>Derive an expression for PN junction diode current under forward bias condition.</td><td>10 Marks</td><td>L3</td><td>CO2</td></tr>
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<table>
<tr><td>13.</td><td>a.</td><td>Explain the construction and working principle of a Schottky diode along with its advantages.</td><td>10 Marks</td><td>L3</td><td>CO3</td></tr>
<tr><td></td><td>b.</td><td>Explain the construction and working principle of BJT Transistors.</td><td>10 Marks</td><td>L3</td><td>CO4</td></tr>
<tr><td colspan="6">Or</td></tr>
<tr><td>14.</td><td>a.</td><td>Describe the working principle of solar cell which helps to convert sunlight into electrical energy.</td><td>10 Marks</td><td>L3</td><td>CO3</td></tr>
<tr><td></td><td>b.</td><td>Explain the IV Characteristics of BJT Transistor.</td><td>10 Marks</td><td>L3</td><td>CO4</td></tr>
</table>

<table>
<tr><td>15.</td><td>a.</td><td>Draw and explain the Ebers–Moll equivalent circuit for an NPN transistor.</td><td>10 Marks</td><td>L3</td><td>CO4</td></tr>
<tr><td></td><td>b.</td><td>Explain with various regions Qualitative operations of E-mode NMOS transistor.</td><td>10 Marks</td><td>L4</td><td>CO5</td></tr>
<tr><td colspan="6">Or</td></tr>
</table>

16.	**a.**	Explain with circuit diagram the basic applications of BJT Transistor.	**10 Marks**	**L3**	**CO4**
	b.	Consider a MOS capacitor with t_{ox} = 200 $\dot{A}$ p-type substrate with acceptor concentration N_a =5 x 10^{16} cm^{-3}. Find the electric field in the oxide and the charge per unit area in the silicon substrate (units C/cm^2) for V_{GB} = -2.5 V.	**10 Marks**	**L4**	**CO5**

17.	**a.**	Explain the statics analysis of CMOS NAND gate.	**10 Marks**	**L3**	**CO6**
	b.	Implement the following Boolean expressions using NMOS & CMOS technology I) Y1 = $\overline{\mathrm{AB} + (\mathrm{C} + \mathrm{D})}$ II) Y2 = $\mathrm{BC} + (\mathrm{E} + \mathrm{D})\mathrm{A}$	**10 Marks**	**L3**	**CO6**
Or					
18.	**a.**	Draw and explain the functioning of 4bit x 4 bit NOR based ROM array.	**10 Marks**	**L3**	**CO6**
	b.	Draw and explain the operation of full CMOS static RAM cell.	**10 Marks**	**L3**	**CO6**