Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

End - Term Examinations – December 2025

Date: 15-12-2025 **Time:** 1.00pm to 04.00pm

School: SOE	**Program:** B. Tech- ECE/ B. Tech- VLSI	
Course Code: ECE3167	**Course Name:** VLSI Design	
Semester: V	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**	**CO6**
Marks	**12**	**12**	**14**	**12**	**24**	**26**

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1.	Illustrate Body Effect	**2 Marks**	**L1**	**CO1**
2.	List out the Advantages of BICMOS.	**2 Marks**	**L1**	**CO2**
3.	Mention PMOS transistor representation in Layout diagram.	**2 Marks**	**L1**	**CO3**
4.	What are the needs of current mirror circuit?	**2 Marks**	**L1**	**CO3**
5.	Draw the small signal model of CS amplifier-Source degeneration circuit.	**2 Marks**	**L2**	**CO4**
6.	Differentiate an ideal op amp and practical op amp.	**2 Marks**	**L1**	**CO5**
7.	Draw the Schematic structure of CMOS folded cascode amplifier	**2 Marks**	**L2**	**CO5**
8.	Illustrate semi-custom ASIC.	**2 Marks**	**L1**	**CO6**
9.	What is system partitioning?	**2 Marks**	**L1**	**CO6**
10.	What are specifications-based Testing?	**2 Marks**	**L1**	**CO6**

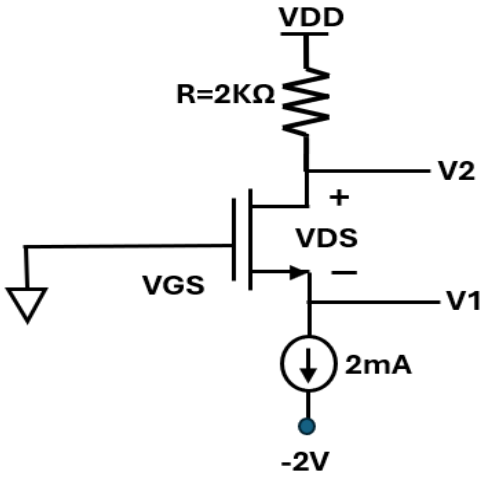
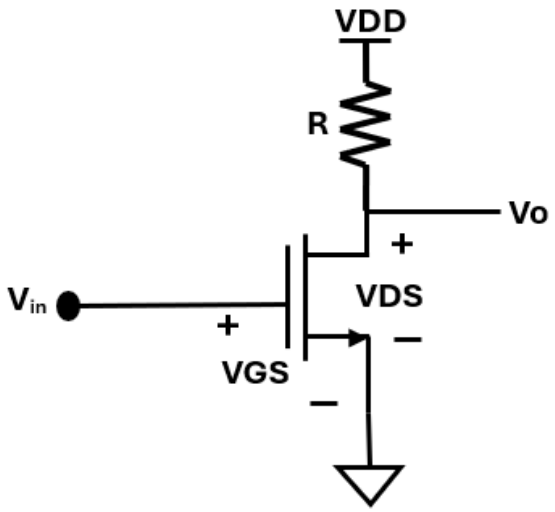
Part B

Answer the Questions. **Total Marks 80M**

11.	**a.**	MOSFETs are widely used in both digital and analog electronics due to their small size and high speed. Explain MOSFET three modes of operation with neat diagrams.	**10 Marks**	**L2**	**CO1**
	b.	Common-drain amplifiers are very useful in CMOS design due to its low output impedance and high input impedance. Describe common drain amplifier.	**10 Marks**	**L2**	**CO4**
		Or			
12.	**a.**	MOS is a voltage-controlled device with three main terminals, and it has various capacitance between terminals and substrate. Explain MOS device capacitance.	**10 Marks**	**L2**	**CO1**
	b.	A common-source (CS) MOSFET amplifier is a circuit where the input signal is applied to the gate, the output is taken from the drain, and the source is common to both the input and output, typically grounded. Describe common source amplifier.	**10 Marks**	**L2**	**CO4**

13.	**a.**	Layout design refers to the arrangement of components in an integrated circuit for fabrication, governed by layout design rules. Design y=(A.(B+C))' using CMOS technology and draw the layout of same using Euler's path.	**10 Marks**	**L3**	**CO2**
	b.	A CMOS inverter is a very simple circuit, designed with two opposite-polarity MOSFETs within a complementary way. Discuss VTC of CMOS Inverter.	**10 Marks**	**L2**	**CO3**
		Or			
14.	**a.**	In CMOS VLSI design, current and voltage references are circuits that provide stable, constant current (IREF) and voltage (VREF) that are insensitive to supply voltage and temperature variations. Describe Supply Independent Biasing- Current Reference.	**10 Marks**	**L3**	**CO3**
	b.	Layout diagrams specify the width of the layers or the spacing between them. Draw the layout of two input CMOS NAND.	**10 Marks**	**L2**	**CO2**

15.	**a.**	The circuit is shown in the figure below, the transistors are characterized by Vt=1V, K'(W/L) =4ma/V2, λ=0. Find the voltage gm, Av, V1 and V2.	**10 Marks**	**L3**	**CO5**

					
	b.	Differential Amplifier produces an output voltage that is proportional to the voltage difference (subtraction) between its two input signals. Explain the differential amplifier's Common mode and differential mode operations.	**10 Marks**	**L2**	**CO5**
		Or			
16.	**a.**	MOSFET is shown in Fig below, Vt=0.4, Kn'=500μA/V2 and λ=0. Find the required values (W/L) and R so that when Vi=VDD=1.3V, rDS=50Ω and V0=50mV. 	**10 Marks**	**L3**	**CO5**
	b.	Differential Amplifier produces an output voltage that is proportional to the voltage difference (subtraction) between its two input signals. Describe differential amplifier's small signal model and gain of the amplifier.	**10 Marks**	**L2**	**CO5**

17.	**a.**	ASIC design is the specialized process of developing integrated circuits (ICs) that are custom-built for a specific application, product, or use case. Describe ASIC design process.	**10 Marks**	**L2**	**CO6**

	b.	The power consumed in a VLSI circuit can be broadly classified into two types – Static power dissipation and Dynamic power dissipation. Describe any two sources of power dissipation.	**10 Marks**	**L2**	**CO6**
		Or			
18.	**a.**	Routing is the process of creating physical connections between or among the signal pins using metal layers. Explain in detail about "Rooting" and its types.	**10 Marks**	**L2**	**CO6**
	b.	A current-mode circuit is a circuit that processes current signals. Explain basic feedback inverting and non-inverting integrators and its advantages.	**10 Marks**	**L2**	**CO6**