Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

Make-up Examinations – December 2025

Date: 29- 12- 2025 **Time:** 01:00pm – 04:00pm

School: SOE	**Program:** B.Tech	
Course Code : ECE3090	**Course Name :** Verilog design	
Semester: MK	**Max Marks**:100	**Weightage**:50%

CO - Levels	**CO1**	**CO2**	**CO3**	**CO4**	**CO5**
Marks	**6**	**30**	**40**	**40**	**---**

Instructions:

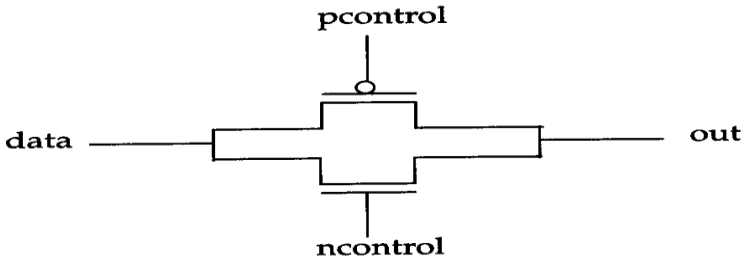
(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1	Draw the circuit for the following keyword of Verilog “buffif0” and “notif0”.	2 Marks	L2	CO1
2	Verilog has 12 primitives using gate level modelling. Write a instantiation of AND gate and nor primitive.	2 Marks	L2	CO2
3	Behavioral modeling in Verilog is described by specifying a set of concurrently active procedural blocks. Name the two procedural blocks in behavioral modelling.	2 Marks	L2	CO3
4	Define net and wire data types in Verilog with one example	2 Marks	L2	CO1
5	Module defines the architecture of hardware to be designed. Define a module for a SR latch with enable.	2 Marks	L2	CO2
6	In Verilog, cmos switch shown below can be instantiated as. Write a syntax by using switch level instantiation.	2 Marks	L2	CO2

				
7	In Verilog, the always block is a fundamental construct used to describe behavior that repeats indefinitely or is triggered by certain events. Write two examples of event using clock to control always block.	2 Marks	L3	CO3
8	Complete the given code of line described using behavioral always block always @(In0 or In1 or In2 or In3 or Sel) begin case (Sel) -----: Out = In0; ----- : Out = In1; 2'b10 : Out = In2; ------ : Out = -----; endcase	2 Marks	L2	CO3
9	The conditional operator ensures decisions are made at high speed within pipelines, making it an efficient construct for processing data streams. Using assign statement write a continuous statement for half adder.	2 Marks	L2	CO1
10	Reusability of the code is crucial in hardware design. Explain the parameters and their types in Verilog.	2 Marks	L2	CO3

Part B

Answer the Questions **Total 80 Marks**

11.	a.	Number of statements within procedural blocks which control the way that signals are assigned are known as sequential statement. The case statement and the if statement are both examples of sequential statements in Verilog. Design a 8:1 multiplexer using this procedural statement.	10 Marks	L3	CO3

or

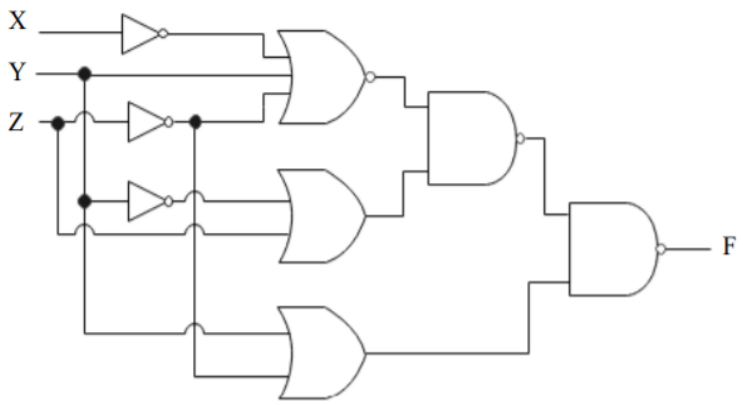
12.	a.	Number of statements within procedural blocks which control the way that signals are assigned are known as sequential statement. The case statement and the if statement are both examples of procedural statements in Verilog. Design a 3:8 decoders using this sequential statement.	10 Marks	L3	CO3

13.	a.	User Defined Primitives (UDPs) in Verilog are custom building blocks that extend the functionality of standard Verilog primitives. They	10 Marks	L3	CO3

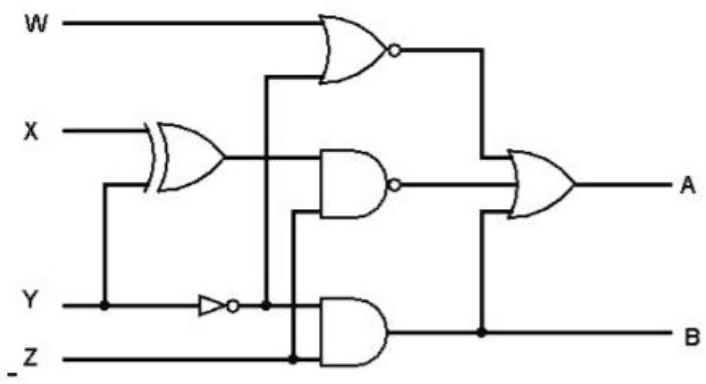
		allow designers to create specialized, reusable components that can encapsulate complex logic or operations. 1. Design a combinational UDP for adding 2 bits a and b 2. Design sequential UDP for latch.			

or

14.	a.	In data flow modelling the keyword "assign" is used to define the output of a circuit and in gate level/switch level primitives are used 1. Develop the 2 input NOR gate using dataflow style of modelling and write a test bench to test the same 2. Draw transistor level schematic for 2 input NOR and write a Verilog code for same	10 Marks	L3	CO2

15.	a.	A combinational circuit is a type of logic where each output depends only on its present input. For the combinational circuit shown below, write the Gate Level (Structural) Verilog description. Make sure that the internal and external signals are properly labeled.  	10 Marks	L3	CO2

Or

16.	a.	A combinational circuit is a type of logic where each output depends only on its present input. For the combinational circuit shown below, write the Gate Level (Structural) Verilog description. Make sure that the internal and external signals are properly labeled.  	10 Marks	L3	CO2

17.	a.	Explain with syntax of the following sequential statements in Verilog. i) For-loop ii) While-loop iii) Repeat iv) Forever. Design a 4-bit shift register using a For loop and while loop	15 Marks	L3	CO3

Or

18.	a.	A function or task is a group of statements that performs some specific action. Both of them can be called at various points to perform a certain operation. They are also used to break large code into smaller pieces to make it easier to read and debug. 1. Explain the difference between function and task. 2. Write a Verilog code for counting numbers of ones in a nibble 1011.	15 Marks	L3	CO3

19.	a.	Behavioral modeling enables you to describe a system at a high level of abstraction. Design a full adder circuit using a behavioral style of modelling using if else statement and verify the same using test bench.	15 Marks	L3	CO3

Or

20.	a.	Behavioral modeling enables you to describe a system at a high level of abstraction. Design a 4 bit shift register circuit using a behavioral style of modelling using model instantiation and write a test bench for the same.	15 Marks	L3	CO3

21.	a.	Develop state diagram for a "1101" sequence detector. This sequence detector will examine a string of 0's and 1's applied to the input x and generate an output z=1 only when the input sequence ends in 1101. The input x can change only between clock active edges. The detector can be designed as either a Mealy FSM. If the sequence detector is designed as a Mealy FSM, the output z=1 coincides with the last 1 in "101 A. Draw a state diagram for the same B. Draw a state table C. Write a Verilog code for the same	20 Marks	L4	CO

Or

22.	a.	Develop state diagram for a "1011" sequence detector. This sequence detector will examine a string of 0's and 1's applied to the input x and generate an output z=1 only when the input sequence ends in 101. The input x can change only between clock active edges. If the detector is designed as a Moore FSM, the output z=1 coincides with the clock edge during the last 1 in "101", typically behind the Mealy output. A. Draw a state diagram for the same B. Draw a state table C. Write a Verilog code for the same	20 Marks	L4	CO4