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PRESIDENCY UNIVERSITY

BENGALURU

Make Up Examinations – December 2025

Date: 26 – 12- 2025

Time: 1.00pm to 04.00pm

School: SOE	Program: B.Tech		
Course Code : ECE3050	Course Name: Design for Testability		
Semester: MK	Max Marks:100	Weightage:50%	

CO - Levels	C01	C02	C03	C04
Marks	24	26	24	26

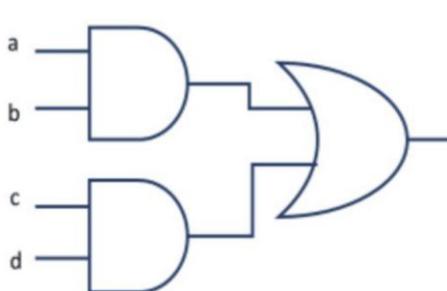
Instructions:

- (i) Read all questions carefully and answer accordingly.
- (ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks.

10Q x 2M=20M

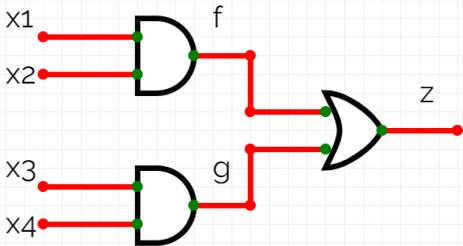
1	How many single stuck-at faults are present in the below combinational circuit? 	2 Marks	L1	CO1
2	Test engineers usually have to construct test vectors after the design is completed. Integration of design and test, referred to as design for testability (DFT), was proposed in the 1970s. List out the Categories of DFT techniques?	2 Marks	L1	CO2

3	What is the significance of Lock up latch in digital design testing?	2 Marks	L1	C03
4	Name two test vector generation techniques for detecting only single faults but not multiple faults?	2 Marks	L1	C02
5	To quantify of the ease of testing two terms are commonly used in DFT i.e controllable and Observable. Define what is controllability and Observability?	2 Marks	L1	C02
6	What are the different types of fault classes?	2 Marks	L1	C04
7	Define primitive polynomial with an example.	2 Marks	L1	C04
8	Define and generate singular cover for EX-OR gate	2 Marks	L1	C01
9	What is goal of DFT Engineer?	2 Marks	L1	C03
10	What is ATE? What it does?	2 Marks	L1	C04

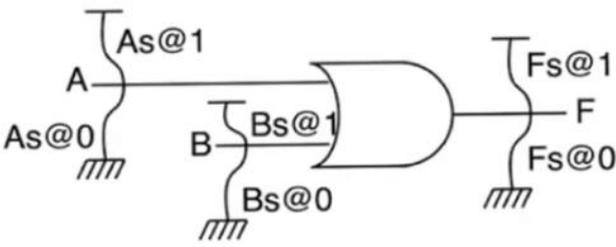
Part B

Answer the Questions

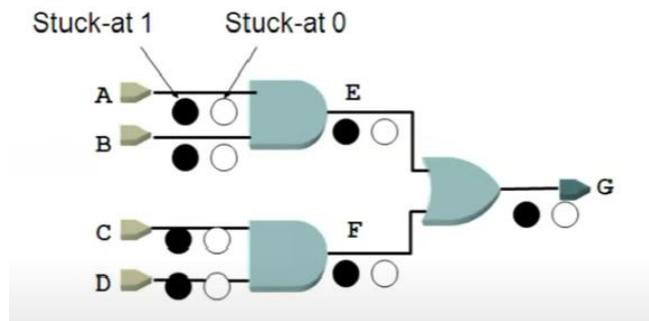
Total 80 Marks.

11.	a.	<p>Generate the test vector for finding SA0 fault on line x1 of the following figure using Boolean difference method with all simplification steps to be mentioned?</p> 	20 Marks	L3	C01
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Or

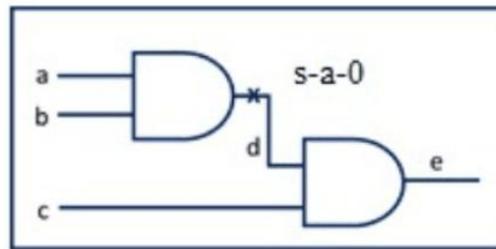
12.	a.	<p>i) a. Find the test vector to be generated to detect faults at the input(A,B) and output(F) pf the OR gate which are stuck at 0 and 1 in the given circuit.</p> 	5+5+5+5 Marks	L2	C01
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ii) Design truth tables for the fault-free circuit and the faulty circuits for all possible single stuck-at faults.



iii) Elaborate on typical defects in VLSI chips with examples.

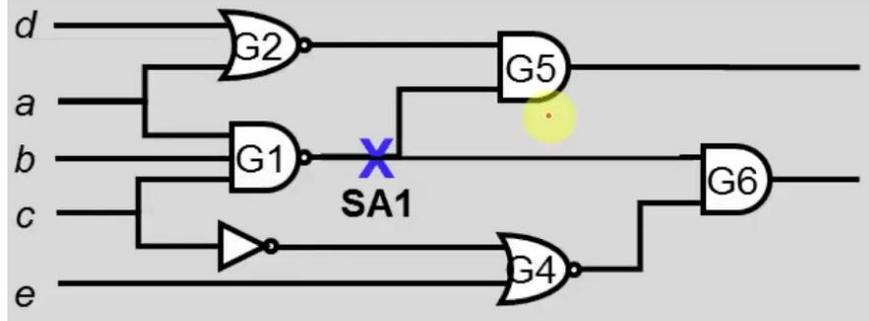
iv) Find the test vector to be generated to detect stuck at 0 faults at net 'd' in the given circuit



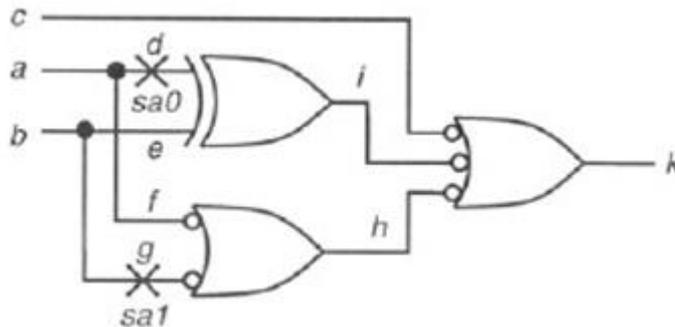
13.	a.	<p>i) Scan cell design is the most widely used structured DFT methodology. Explain about Edge triggered Muxed D Scan Cell design and test operation with suitable diagrams and waveforms?</p> <p>ii) In VLSI engineering a common fault after stuck at fault model is a bridging fault. Discuss the different types of bridging faults with an example.</p>	(10+10) Marks	L2	CO2
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Or

14.	a.	<p>i) How the path sensitization method is used to generate a test pattern for combinational circuits? Find the test vector using path sensitization method for the given figure.</p>	(10+10) Marks	L3	CO2
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ii) Find the test vector for the given figure using truth table for faulty and fault free circuit



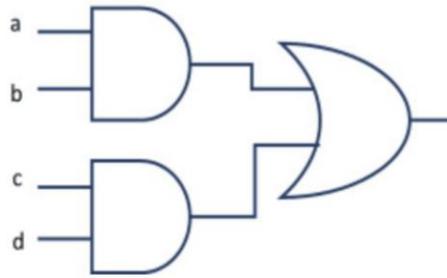
15.	a.	<p>i) An automated test pattern generator called Built-in Self-Test(BIST) is utilized to find faults. Discuss the BIST logic system architecture?</p> <p>ii) What is the advantage of pseudo exhaustive pattern generator over exhaustive pattern generator?</p> <p>iii) Write a note on ad hoc DFT methods.</p> <p>iv) Explain why BIST is the preferred form of DFT?</p>	5+5+5+5 Marks	L2	C03
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Or

16.	a.	<p>i) Scan Compression is a DFT technique that reduces the testing time. Discuss the importance of scan compression technique with neat block diagram.</p> <p>ii) Discuss the economic case for BIST using some chip level testability problems.</p>	(10+10) Marks	L2	C03
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17.	a.	<p>i) Write a detail description about LFSR types and properties with a neat sketch? Generate the test sequence using given characteristic polynomial $X^5 + X^3 + X + 1$?</p>	(10+10) Marks	L3	C04
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ii) Write about signature analysis / Transition count response compaction with a neat sketch for given circuit faulty and fault free circuit where $a=10101$ $b=10100$ $c=11100$ $d=10100$ considering SA0 fault on line b.

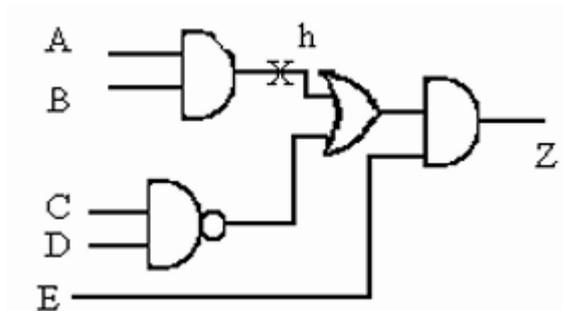


Or

18.

i) Explain the steps in D algorithm? Generate the test vector for SA1 fault on the line h as shown in figure using D-algorithm?

a.



20
Marks

L3 CO4

***** BEST WISHES *****