Roll No												

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

Make-Up Examinations DECEMBER-2025

Semester: MK

Course Code: ECE3048

Course Name: FPGS Design for embedded system

Program: B Tech

Date: 27-12-2025

Time: 01:00 PM-04:00 PM

Max Marks: 100

Weightage: 50 %

Instructions:

(i) Read the all questions carefully and answer accordingly.

(ii) Do not write any matter on the question paper other than roll number.

Part A [Memory Recall Questions]

Answer all the Questions. Each question carries Two marks. (5Qx 4M= 20M)

1. Data types in Verilog inform the compiler whether to act as a transmission line (like a wire) or store data. Describe the data types NET and REG with example ?

(C.O.No.2)[Knowledge Level]

2. If we need a little logic to implement, we will choose CPLD and for a complex function we will use FPGA. There are many markets player to provide the solution for the same. Mention four popular vendors who provide FPGA.?

(C.O.No.1)[Knowledge Level]

3. Configurable logic block makes FPGA more suitable choice for the designer. Explain various components of these programable blocks.

(C.O.No.2)[Knowledge Level]

4. In competitive environment, chip development cycles are compressed, causing design teams to reuse semiconductor Intellectual Property (IP) to accelerate time to market. List the types of Ip core available and classify them correctly?

(**C.O.No.3)[Knowledge Level]**

5. The first programable logic device was developed in 1956 and commercially made available in 1971. List all this logic device and draw any one structure in detail?

(C.O.No.1)[Knowledge Level]

Part B [Thought Provoking Questions]

Answer all the Questions. Each question carries Ten marks. (5Qx10M=50M)

6. PLA and PAL are part of SPLD and also contribute to the development of CPLD family devices in earlier generations. Implement the given Boolean equation using PAL and PLA. As per implementation suggest your comment on each design. F=AB'+AC'B+B'C' **(C.O.No1)[Comprehensive Level]**

7. A lookup table (LUT) is a characteristic feature of an FPGA. A LUT stores a predefined list of logic outputs for any combination of inputs. Here there are four variables A,B,C,D and the available LUT size is 3 input LUT . The output becomes high only when any of the two input variables (A,B,C,D) are one.
1. Is it possible to implement the boolean expression[1]
2. Design a truth table for the same.[1]
3. Show how the values will be stored in LUT [2]
4 Now, if ABCD = 0101, then show the output of the LUT, Y, will take what value from the ----------memory cell and makes its way to the output [6]

8. The FPGA dominates the programable logic world and most importantly, it also helps to develop fast solutions for the Embedded designs.
(a) Discuss various types of types FPGAs [6]
(b) List out all the components of FPGA.

9. Hardware description language plays a role in deciding the target FPGA device for design.
(a) List various styles of modeling as per Y chart of the modeling [4]
(b) If you have been asked to design combinational logic shown below using Verilog, Which method you will select and also write Verilog code using that method

(C.O.No.1)[Comprehensive Level]

10. Once we create soft core processor, most important part is programming a soft-core processor.
(a) Mention various software platforms available to programme softcore processor. [2]
(b) Name software interface available in Quartus prime to program soft core processor. [2]
(c) List the difference between embedded programming and application programming for embedded systems. [6]

C.O.No.3) [Comprehensive Level]

Part C [Problem Solving Questions]

Answer all the Questions. Each question carries Twenty marks. (2Qx15M=30M)

11. Embedded processor are classified into two different class based on the data and instruction they access from the memory known as RISC and CISC processor?
A. List the basic difference between RISC and CISC processor? [4]
B. List various applications where they use embedded processors?[4]
C. Name the operating systems supported by embedded processor [2]
D. FPGA are becoming a first choice to implement the design, discuss the components and IP available in FPGA that makes it a better choice [5]

(C.O.No.3)[Application Level].

12. To EDA tools helps to create VLSI design in reality and also make it easy job to handle the Timing constraints and RTL design. These tools need to follow a systematic design flow of to achieve the great design. If you are a VLSI designer and you have been asked to create a prototype of the device

List various design modelling styles used in VLSI design?[3]

Explain the VLSI design flow in detail to final implementation on FPGA?[12]

(**C.O.No.)[Comprehensive Level**].