| Roll No. | | | | | | | | | | | | |
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# PRESIDENCY UNIVERSITY

## BENGALURU

**Make Up Examinations – December 2025**

**Date:** 26 – 12- 2025 **Time:** 9:30am – 12:30pm

| | | |
|---|---|---|
| **School:** SOE | **Program:** ECE(VLSI) | |
| **Course Code :** ECE2013 | **Course Name :** Digital System Design Using HDL | |
| **Semester**: MK | **Max Marks**:100 | **Weightage**: 50% |

| **CO - Levels** | **CO1** | **CO2** | **CO3** | **CO4** | **CO5** |
|---|---|---|---|---|---|
| **Marks** | **24** | **28** | **24** | **24** | **--** |

**Instructions:**

*(i) Read all questions carefully and answer accordingly.*

*(ii) Do not write anything on the question paper other than roll number.*

## Part A

**Answer ALL the Questions. Each question carries 2marks.** **10Q x 2M=20M**

| | | | | |
|---|---|---|---|---|
| **1** | What does VHDL and Verilog stand for? | **2 Marks** | **R** | **CO1** |
| **2** | What is the difference between Net and register | **2 Marks** | **R** | **CO1** |
| **3** | Declare a memory of size 512 * 4 in Verilog | **2 Marks** | **U** | **CO4** |
| **4** | Declare a net variable *a_x* which is a 8 bit vector in verilog | **2 Marks** | **U** | **CO2** |
| **5** | What is the output for expressions given A= 3'b010, b = 3'b100, c=4'b1101<br>Y = 2{a[1], b, c[3]} | **2 Marks** | **U** | **CO2** |
| **6** | The other name for CBIC is _____ | **2 Marks** | **R** | **CO3** |
| **7** | What are the different hazard types in combinational networks | **2 Marks** | **R** | **CO3** |
| **8** | What is the difference between 1 bit overlap and non overlap with example | **2 Marks** | **U** | **CO2** |
| **9** | What is the difference between ROM, PAL and PLA | **2 Marks** | **R** | **CO4** |
| **10** | Differentiate between Mealy and Moore FSM | **2 Marks** | **2** | **CO2** |

## Part B

**Answer the Questions** **Total 80 Marks.**

| | | | | | |
|---|---|---|---|---|---|
| **11.** | **a.** | Why is Verilog popular? What are its features? | **10 Marks** | **R** | **CO1** |
| | **b.** | Explain the top down and bottom up approach in IC design methodologies | **10 Marks** | | |
| | | **Or** | | | |
| **12.** | **a.** | Write a Verilog code to implement SR flip Flop and JK flip flop using gate level modelling style | **10 Marks** | **U** | **CO1** |
| | **b.** | Explain with example the following Verilog operators<br>1. Conditional operator<br>2. Logical operators | **10 Marks** | | |
| **13.** | **a.** | Implement a Half Subtractor circuit using gate level, data flow and behavioral styles. Write any one test bench code to verify the output additionally draw the expected output waveforms according to the test bench code | **20 Marks** | **U** | **CO2** |
| | | **Or** | | | |
| **14.** | **a.** | Develop a sequence detector to detect a sequence 0110 with no overlap using Mealy and Moore style. | **10 Marks** | **A** | **CO2** |
| | **b.** | Write the Verilog design code and the test bench code for the above sequence detector (for any one) | **10 Marks** | | |
| **15.** | **a.** | Build a full adder circuit using an ROM IC of size 8*2. Identify the number of input and outputs. How many words can be stored in the ROM memory and what is the size of each word? | **10 Marks** | **A** | **CO4** |
| | **b.** | Implement F1 = ∑m(0,1,3,7) F2 = ∑m(1,4) F3 = ∑m(0,2) using programmable array logic(PAL) | **10 Marks** | | |
| | | Or | | | |
| **16.** | **a.** | With a neat figure explain the working of Binary Divider? Perform the operation 135 / 13. Show all steps for division. | **20 Marks** | **A** | **CO4** |
| **17.** | **a.** | With a neat figure explain the IC design and development cycle using Y chart | **14 Marks** | **R** | **CO3** |
| | **b.** | What are the 3 major design hierarchies in IC design | **6 Marks** | | |
| | | **Or** | | | |
| **18.** | **a.** | Differentiate between Full custom IC design and Semi-custom IC design | **10 Marks** | **R** | **CO 3** |
| | **b.** | Write a note on classification of semi-custom IC design | **10 Marks** | | |