Roll No.												

PRESIDENCY UNIVERSITY

BENGALURU

Make up Examinations – December 2025

Date: 31 – 12- 2025 **Time:** 09:30am – 12:30pm

School: SOE	**Program:** B Tech-VLSI	
Course Code : ECE2012	**Course Name :** Solid State Electronics	
Semester: MK	**Max Marks**: 100	**Weightage**: 50%

CO - Levels	CO1	CO2	CO3	CO4	CO5
Marks	10	10	20	30	30

Instructions:

(i) Read all questions carefully and answer accordingly.

(ii) Do not write anything on the question paper other than roll number.

Part A

Answer ALL the Questions. Each question carries 2marks. **10Q x 2M=20M**

1	Identify the quantum mechanical phenomenon in which an object such as an electron or atom passes through a potential energy barrier that, according to classical mechanics, should not be passable due to the object not having sufficient energy to pass or surmount the barrier.	**2 Marks**	**L1**	**CO2**
2	The way the atoms are bonded, in a NaCl is different from that of a Carbon. Name the type of bonding in NaCl and Carbon.	**2 Marks**	**L1**	**CO2**
3	In any material, the Pauli's exclusion principle plays an important role in bandgap formation. State Pauli's exclusion principle.	**2 Marks**	**L1**	**CO2**
4	John observed that if same electric field is applied to an electron in vacuum and in a crystal, it accelerates with different velocities. Why?	**2 Marks**	**L1**	**CO2**
5	At thermal equilibrium, the electron and hole concentration relationship is given by the mass action law. Write mathematically the expression for the mass action law.	**2 Marks**	**L1**	**CO2**

6	A Field Effect Transistor is a unipolar transistor with three terminals. Name the three terminals of a JFET.	**2 Marks**	**L1**	**CO5**
7	Billions of MOS transistors are used, together in semiconductor memory devices and microprocessors. List any two features of Field Effect Transistor that enable them for above application.	**2 Marks**	**L1**	**CO5**
8	In any FETs, the width of the channel can be controlled, by applying a voltage to the gate, which in turn controls the current flowing from the source to the drain. Identify the gate voltage at which the drain current reaches the saturation value.	**2 Marks**	**L1**	**CO5**
9	Shorter channels experience a reduction in the effective channel length as V_{DS} increases, leading to a rise in I_D even in saturation. Write the equation for the modified saturation current for a short channel MOSFET.	**2 Marks**	**L1**	**CO5**
10	2DEG(2 Dimensional Electron Gas) is formed at the interface of the materials due to differences in their band gaps. This 2DEG acts as a high-mobility electron channel for current flow. In which type of transistor 2DEG is commonly seen?	**2 Marks**	**L1**	**CO5**

Part B

Answer the Questions **Total 80 Marks**

11.	**a.**	LEDs use direct band semiconductors whereas for the making of transistors, indirect band semiconductors are used. Is the above statement true? Explain with necessary diagrams the various types of semiconductors based on band gap.	**10 Marks**	**L2**	**CO1**

Or

12.	**a.**	In solids, the formation of a bandgap is directly linked to the Pauli exclusion principle. Explain the formation of bandgap in Carbon with the help of a neat diagram.	**10 Marks**	**L2**	**CO1**

13.	**a.**	Zener breakdown typically occurs at lower voltages (around 5 volts or less), while avalanche breakdown happens at higher voltages exceeding that range; meaning the voltage above which both breakdown types occur is considered to be around 5 volts and higher where the avalanche effect becomes dominant. Explain the breakdown processes in a p-n junction diode with necessary diagrams.	**10 Marks**	**L2**	**CO3**

Or

14.	**a.**	Consider a Silicon pn junction at room temperature doped at $N_a=10^{16}/cm^3$ in the p region and $N_d=10^{17}/cm^3$ in the n region. Intrinsic carrier density is $1.5x10^{10}/cm^3$ at room temperature. Find the barrier potential and width of the depletion region. For Si the permittivity is given as $1.04x10^{-12}$ F/cm, Charge of an electron $1.6x10^{-19}$C.	**10 Marks**	**L2**	**CO3**
15.	**a.**	According to Quantum mechanics, there is a finite probability that carriers can penetrate through the barrier of thin width. Explain the diode working on above phenomenon.	**10 Marks**	**L2**	**CO3**
		Or			
16.	**a.**	A metal-semiconductor junction is formed when a metal comes into contact with a semiconductor material. Explain the various types with necessary diagrams.	**10 Marks**	**L2**	**CO3**
17.	**a.**	Unlike conventional Bipolar Junction Transistors (BJTs), HBTs use different semiconductor materials for the emitter and base regions, which gives them unique advantages. Explain about Heterojunction Bipolar transistors.	**15 Marks**	**L2**	**CO4**
		Or			
18.	**a.**	A transistor is an important solid state electronic device used in amplification and switching applications. Explain the operation of BJT with the help of p-n-p transistor and derive the amplification factor β.	**15 Marks**	**L2**	**CO4**
19.	**a.**	The Early effect is a phenomenon that occurs in bipolar junction transistors (BJTs) when the effective width of the base changes due to a variation in the base-to-collector voltage. Discuss how the base width variation affects the normal working of a BJT.	**15 Marks**	**L2**	**CO4**
		Or			
20.	**a.**	The current gain of a BJT decreases at high collector current. Is the above statement true? Justify your answer with necessary explanations and diagrams.	**15 Marks**	**L2**	**CO4**
21.	**a.**	Metal Oxide Semiconductor Field Effect Transistors are voltage-controlled devices, in which a metal electrode placed on top of an insulator (typically SiO2) on the silicon surface, is used to control the flow of current between two ohmic contacts on the silicon. Explain the working of MOSFET with necessary diagrams and equations.	**20 Marks**	**L2**	**CO5**
		Or			

22.	**a.**	CMOS is based on metal-oxide semiconductor field-effect transistor (MOSFET) technology, which uses switches or amplifiers to control the amount of electricity flowing between terminals. Explain the various processes involved in CMOS fabrication with necessary diagrams and the working of a CMOS technology based inverter.	**20 Marks**	**L2**	**CO5**

******* BEST WISHES *******